CMS32M55xx Reference manual

Enhanced flash 32-bit motor microcontroller

Rev. 1.11

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1. ARM Cortex–M0 core

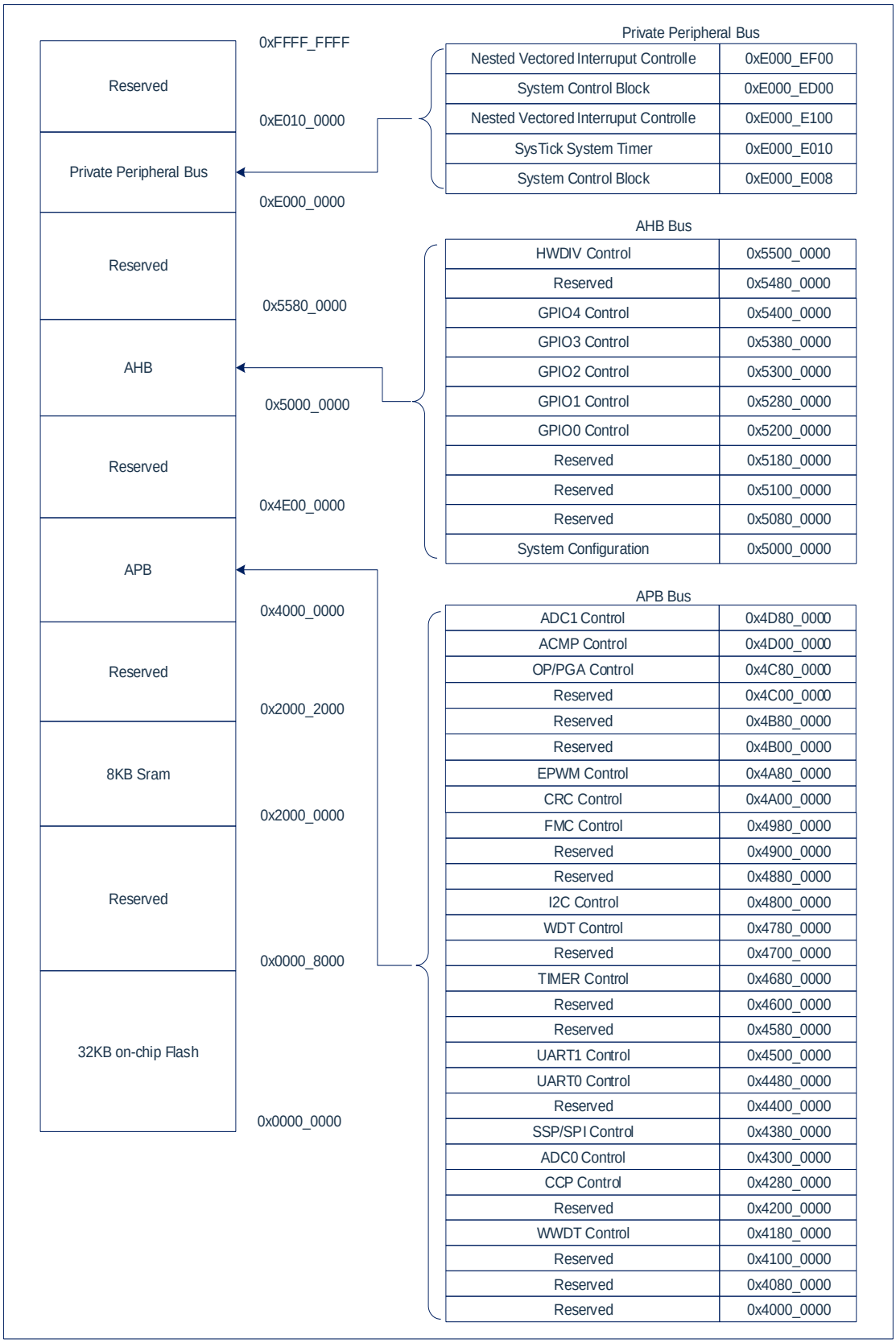
1.1 overview

The Cortex-M0® processor is a configurable, 32-bit RISC processor with multi-stage pipeline. It has an AMBA AHB-Lite interface and includes NVIC components, as well as optional hardware debugging capabilities. The processor can execute Thumb instructions and is compatible with other Cortex-M® series processors. The processor supports two modes of operation – Thread mode and Handler mode. When an exception occurs, the system enters Handler mode, and the exception return can only be performed in Handler mode. You can enter Thread mode after the system resets and the exception returns.

1.2 characteristic

- Low Gate Count Processor:
  - ARMv6-M Thumb® instruction set.
  - Thumb-2 technology.
  - The ARMv6-M is compatible with 24-bit system timers.
  - A 32-bit hardware multiplier.
  - The system interface supports small-endian data access.
  - Accurate and timely interrupt handling capabilities.
  - Loading/storing multiple data and multicycle multiplication instructions can be terminated and then restarted for fast interrupt handling.
  - Exception compatibility mode for the binary interface of the C application.
  - ARMv6-M's C Application Binary Interface (C-ABI) exception compatibility mode allows users to implement interrupt handling using pure C functions.
- NVIC:
  - 32 external interrupts, each with a priority of 4.
  - Dedicated non-maskable interrupts (NDIs).
  - Both level and pulse trigger interrupts are supported.
  - Supports interrupt wake-up controllers (WICs) that provide very low-power idle modes.
- Debugging support:
  - Four hardware breakpoints.
  - Two observation points.
  - Program Count Sampling Register (PCSR) for non-intrusive code analysis.
  - Single-step and vector capture capabilities.
- Bus interface:
  - Provides a simple and integrated single 32-bit AMBA-3 AHB-Lite system interface for all system interfaces and memory.
  - Supports a single 32-bit slave port for DAP (Debug Port).

2. Storage mapping



Note: The above is the largest resource map for this series of products.

3. Clock control

3.1 overview

The clock controller provides a clock source for the entire chip, including the system clock and all peripheral clocks. The controller also controls power consumption through separate clock switches, clock source selection, and a divider.

The clock generator consists of the following two clock sources:

- Internal high-speed oscillator HSI (48MHz/64MHz).
- Internal low speed oscillator LSI (40KHz).

3.2 Feature description

3.2.1 Configure the CLKO feature

- Set the P36 or P35 configuration register to the CLKO function.
- Set the CLKODIV register, select the clock source, and divide the output.
- Enables the CLKO output.

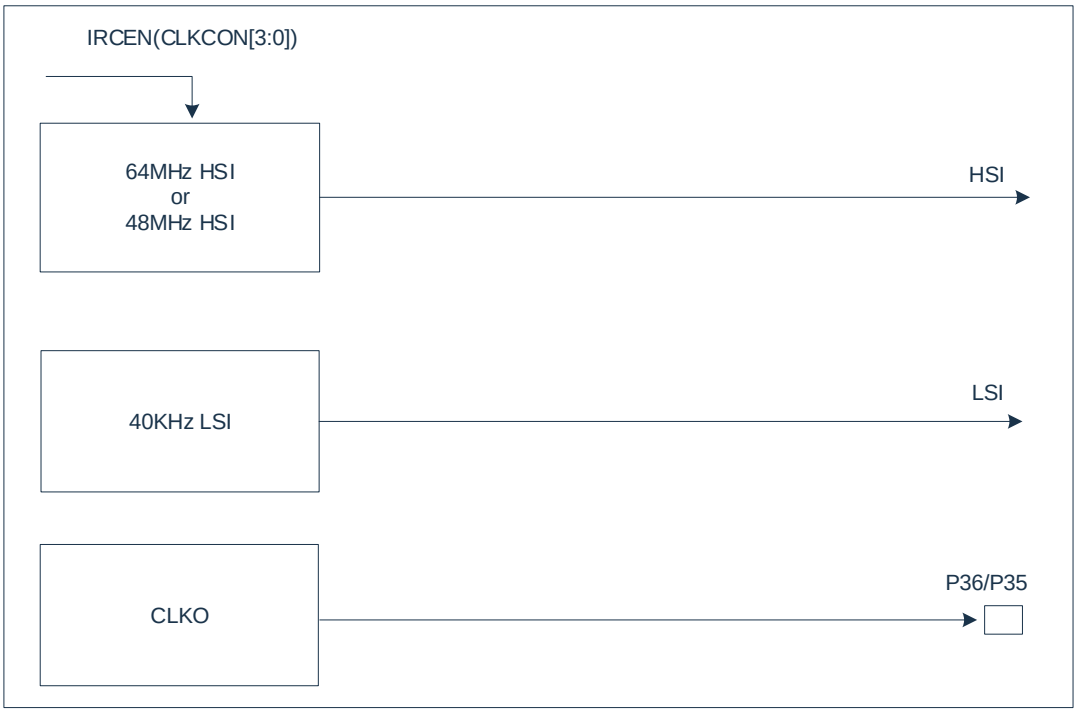


Figure 3-1: Block diagram of the clock structure

3.3 Clock control block diagram

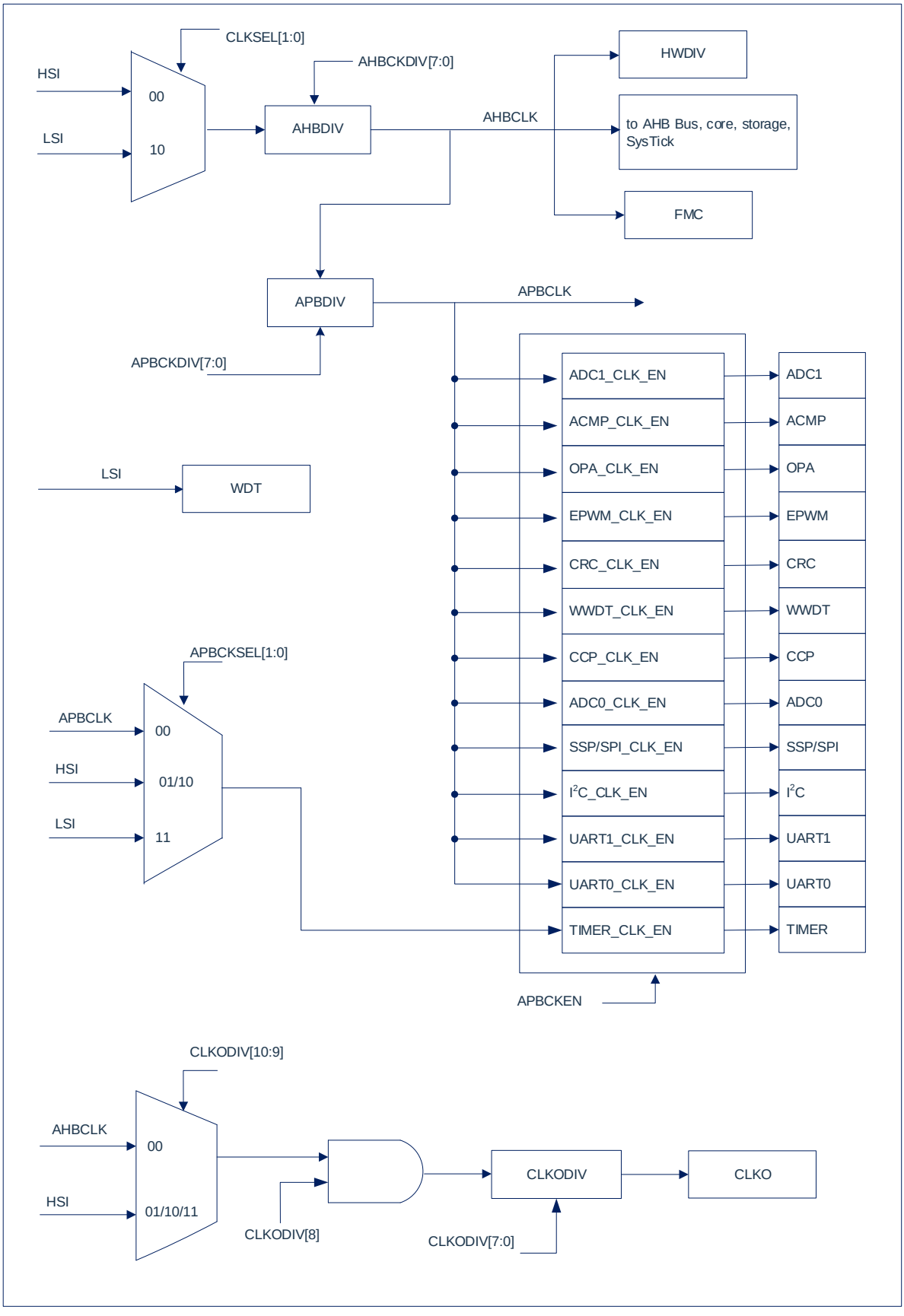


Figure 3-2: Clock control block diagram

4. power management

4.1 overview

The chip has different operating modes to adapt to the power consumption requirements of different applications.

4.2 Working mode

The following table lists the available clocks and wake-up sources in different modes.

	Normal mode	Sleep mode (SCR. SLEEPDEEP=0)	Deep sleep mode (SCR. SLEEPDEEP=1)	Stop mode
definition	The MCU is in normal working condition, peripherals are operating normally, and the LDO is turned on	The MCU is asleep, the CPU stops working, the peripherals are functioning normally, and the LDO is turned on	The MCU is in deep sleep mode, the CPU stops working except for the WDT, and the LDO is turned on	The MCU is in stop mode, all modules stop working, and the LDO is in low-power mode
Entry conditions	The chip is in normal mode after the system reset is complete	The sleep mode enable bit is set and the CPU executes the WFI command	The deep sleep mode enable bit is set and the CPU executes the WFI command	Stop mode enables the bit is set and the CPU executes the WFI command
Wake up the source	-	All interrupts	I/O interrupt,WDT interrupt	I/O interrupts
Available clocks	-	All clocks except AHBCLK	Internal low speed 40KHz clock	not
Post-wake mode	-	The MCU returns to normal mode and the program continues	The MCU returns to normal mode and the program continues	The MCU returns to normal mode and the program continues
Wait time after wake-up	-	Run the program immediately	~25us@Fsys=48MHz	~60us@Fsys=48MHz
External reset	Supported (The reset port is kept low > 100 us reset system).	Supported (The reset port remains low >100us reset system).	Supported (The reset port remains low >100us reset system).	Not supported
Low-voltage reset	Supported	Supported	Not supported	Not supported
Low voltage detection	Supported	Supported	Not supported	Not supported
Low power consumption	-	-	~200uA	~10uA

4.3 Power supply low voltage detection (LVD)

The chip contains a low voltage detection circuit that senses the voltage of the chip's supply pin VDD.

The detected voltage point can be set to: 3.7V/3.0V/2.7V/2.4V/2.2V/2.0V.

5. System Control (SYSCON)

5.1 overview

System control consists of the following sections:

- System reset.
- System power distribution.
- Sleep mode management.
- System management registers for product ID, chip reset, on-chip controller reset, and multifunction pin control.
- System Timer (SysTick).
- Nested interrupt vector controller (NVIC).
- System control registers.

5.2 Register mapping

(SYSCON base address = 0x5000_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
DID	0x000	RO	Product ID register	-
AHBCKDIV	0x004	R/W	AHB clock divider register	0x0
APBCKDIV	0x008	R/W	APB clock divider register	0x0
APBCKEN	0x00C	R/W	The APB clock enable register	0xFFFFFFFF
CLKODIV	0x010	R/W	Clock output control registers	0x0
PCON(P0)	0x014	R/W	Power control registers	0x0
RSTCON(P0)	0x018	WO	Reset control registers	0x0
RSTSTAT	0x01C	R/W	Reset status register	-
CLKCON(P0)	0x020	R/W	The clock source control register	0x2F
CLKSEL(P0)	0x024	R/W	Clock source selection register	0x0
CLKSTAT	0x028	RO	Clock source status register	0x1
APBCKSEL	0x02C	R/W	APB clock source selection register	0x0
IOMUX	0x030	RO	IO multiplexed status register	0xFF
CIDL	0x034	RO	UID[63:32]	-
YES	0x038	RO	UID[95:64]	-
LVDCON	0x03C	R/W	LVD control register	0x0
IOP00CFG(P1A)	0x040	R/W	P00 Configuration register	0x0
IOP01CFG(P1A)	0x044	R/W	P01 Configuration register	0x0
-	0x048	-	Reserved	-
-	0x04C	-	Reserved	-
IOP04CFG(P1A)	0x050	R/W	P04 Configuration register	0x0
IOP05CFG(P1A)	0x054	R/W	P05 Configuration register	0x0
IOP06CFG(P1A)	0x058	R/W	P06 Configuration register	0x0
IOP07CFG(P1A)	0x05C	R/W	P07 Configuration register	0x0
IOP10CFG(P1A)	0x060	R/W	P10 Configuration register	0x0
-	0x064	-	Reserved	-
IOP12CFG(P1A)	0x068	R/W	P12 configuration register	0x0
IOP13CFG(P1A)	0x06C	R/W	P13 configuration register	0x0
IOP14CFG(P1A)	0x070	R/W	P14 Configuration register	0x0
IOP15CFG(P1A)	0x074	R/W	P15 configuration register	0x0

register	Offset	R/W	description	Reset value
IOP16CFG(P1A)	0x078	R/W	P16 Configuration register	0x0
IOP17CFG(P1A)	0x07C	R/W	P17 configuration register	0x0
-	0x080	-	Reserved	-
IOP21CFG(P1A)	0x084	R/W	P21 configuration register	0x0
IOP22CFG(P1A)	0x088	R/W	P22 configuration register	0x0
IOP23CFG(P1A)	0x08C	R/W	P23 configuration register	0x0
IOP24CFG(P1A)	0x090	R/W	P24 configuration register	0x0
IOP25CFG(P1A)	0x094	R/W	P25 configuration register	0x0
IOP26CFG(P1A)	0x098	R/W	P26 configuration register	0x0
-	0x09C	-	Reserved	-
IOP30CFG(P1A)	0x0A0	R/W	P30 configuration register	0x0
IOP31CFG(P1A)	0x0A4	R/W	P31 configuration register	0x0
IOP32CFG(P1A)	0x0A8	R/W	P32 configuration register	0x0
-	0x0AC	-	Reserved	-
IOP34CFG(P1A)	0x0B0	R/W	P34 configuration register	0x0
IOP35CFG(P1A)	0x0B4	R/W	P35 configuration register	0x0
IOP36CFG(P1A)	0x0B8	R/W	P36 configuration register	0x0
-	0x0BC	-	Reserved	-
IOP40CFG(P1A)	0x0C0	R/W	P40 configuration register	0x0
-	0x0C4	-	Reserved	-
-	0x0C8	-	Reserved	-
IOP43CFG(P1A)	CC 0x0	R/W	P43 Configuration register	0x0
IOP44CFG(P1A)	0x0D0	R/W	P44 configuration register	0x0
-	0x0D4	-	Reserved	-
IOP46CFG(P1A)	0x0D8	R/W	P46 Configuration register	0x0
IOP47CFG(P1A)	0x0DC	R/W	P47 Configuration register	0x0
-	--	-	-	-
SYS_IMSC	0x100	R/W	system detect interrupt enable register	0x0
SYS_RIS	0x104	RO	system detect interrupt source status register	0x0
SYS_MIS	0x108	RO	system detect enabled interrupt status register	0x0
SYS_ICLR	0x10C	WO	system detect interrupt clear register	0x0
HSI_TRIM(P0)	0x110	R/W	Internal oscillation frequency trimming register	-
-	-	-	-	-
SRAMLOCK(P0)	0x1B0	R/W	SRAM write-protect register	0x0
GPIO0LOCK	0x1C0	R/W	GPIO0 write enable register	0x0
GPIO1LOCK	0x1C4	R/W	GPIO1 write enable register	0x0
GPIO2LOCK	0x1C8	R/W	GPIO2 write enable register	0x0
GPIO3LOCK	0x1DC	R/W	GPIO3 write enable register	0x0
GPIO4LOCK	0x1D0	R/W	GPIO4 write enable register	0x0
IOCFGLOCK	0x1FC	R/W	Port configuration write enable register	0x0
-	-	-	-	-
UIDX	0x500	RO	UID[31:0]	-
PCRCD	0x510	RO	Program checksum	
UUIDWC0	0x520	CHK	Detect USRID[31:0]	0x0
UUIDWC1	0x524	CHK	Detect USRID[63:32]	0x0
UUIDWC2	0x528	CHK	Detect USRID[95:64]	0x0

register	Offset	R/W	description	Reset value
UUIDWCS	0x52C	CHK	Detect fixed code	0x0

Note:

1) (P0/P1D) The registers labeled are protected registers.
2) (P0): When the marked register writes a valid control bit, other bits need to be written to a fixed value, otherwise the write operation is invalid, see the register description.
3) (P1A): When IOCFGLock=99H, the marked register is allowed to write; = Other values, forbidden to write.

5.3 Register description

5.3.1 Product ID Register (DID)

bit	symbol	description	Reset value
31:16	BOTTOM	Kernel ID	0x4B02
15:0	-	Reserved	-

5.3.2 AHB clock divider register (AHBCKDIV)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	AHBDIV	AHB clock division bits 0: HCLK = F_{SYS} 1~255: HCLK = F_{SYS}/(2×AHBDIV)	0x0

5.3.3 APB clock divider register (APBCKDIV)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	APBDIV	APB clock division bits 0: PCLK = HCLK 1~255: PCLK = HCLK/(2×APBDIV)	0x0

5.3.4 APB Clock Enable Register (APBCKEN).

bit	symbol	description	Reset value
31:28	-	Reserved	-
27	ADC1CE	ADC1 clock enable bit 0: Disable 1: Enable	1
26	ACMPCE	ACMP clock enable bit 0: Disable 1: Enable	1
25	OP/PGACE	OP/PGA clock enable bit 0: Disable 1: Enable	1
24:22	-	Reserved	-
21	EPWMCE	EPWM clock enable bit 0: Disable 1: Enable	1
20	CRCCE	CRC clock enable bit 0: Disable 1: Enable	1
19:15	-	Reserved	-
14	WWDTCE	WWDT clock enable bit 0: Disable 1: Enable	1
13	-	Reserved	-
12	EC SPC	Capture/PWM clock enable bit 0: Disable 1: Enable	1
11	ADC0CE	ADC0 clock enable bit 0: Disable 1: Enable	1
10	-	Reserved	-
9	SSP/SPICE	SSP/SPI clock enable bit 0: Disable 1: Enable	1
8	-	Reserved	-
7	I2CCE	I2C clock enable bit 0: Disable 1: Enable	1
6:5	-	Reserved	-
4	UART1CE	UART1 clock enable bit 0: Disable 1: Enable	1
3	UART0CE	UART0 clock enable bit 0: Disable 1: Enable	1
2	HWDIVCE	HWDIV clock enable bit 0: Disable 1: Enable	1

1	TIMER01CE	TIMER01 clock enable bit 0: Disable 1: Enable	1
0	WDTCE	WDT clock enable bit 0: Disable 1: Enable	1

5.3.5 Clock output control register (CLKODIV)

bit	symbol	description	Reset value
31:11	-	Reserved	-
10:9	CLK_SEL	F_{SEL} clock source select bits 00: AHBCLK 01: HSI 02: HSI 03: HSI	0x0
8	IN	Clock output enable bit 0: Disable CLKO function 1: Enable CLKO function	0x0
7:0	DIV	Clock output divider 0: $F_{CLKO}=F_{SEL}$ 1~255: $F_{CLKO}=F_{SEL}/(2\times DIV)$	0x0

5.3.6 Power Control Register (PCON)

bit	symbol	description	Reset value
31:16	Key	0x5A69 needs to be written at the same time to operate on the other bits of the register	0x0
15:3	-	Must be 0	-
2	Stop mode	Stop mode enable bit 0: Disable stop mode 1: Enable stop mode, execute WFI instructions will enter stop mode	0x0
1	Deep sleep mode	Deep sleep mode enable 0: Disable deep sleep mode 1: Enable Deep sleep mode, and executing WFI instructions will enter deep sleep mode	0x0
0	Sleep mode	Sleep mode enable bit 0: Disable sleep mode 1: Enable sleep mode, and executing WFI instructions will enter sleep mode	0x0

5.3.7 Reset Control Register (RSTCON)

bit	symbol	description	Reset value
31:2	RSTKEY	0x156A99A6 needs to be written at the same time to operate on the other bits of this register, and the read value is 0	0x0
1	CPURST	Write 1 to reset the Cortex-M0 CPU and FMC module (do not load the boot configuration). Writing 0 does not affect	0x0
0	MCURST	Write 1 Reset MCU (Reload Boot Configuration) Writing 0 does not affect	0x0

Note: Write 0x55AA6699 generate MERCUR; Write 0x55AA669A produces CRISP.

5.3.8 Reset Status Register (RSTSTAT)

bit	symbol	description	Reset value
31:3	-	Reserved	-
2	CPURS	CPU reset state 0: No CPU reset detected 1: CPU reset detected	-
1	MCURS	MCU reset status 0: No MCU reset is detected 1: MCU reset detected	-
0	WDTRS	WDT reset status 0: No WDT reset is detected 1: WDT reset detected	-

5.3.9 Clock Source Control Register (CLKCON)

bit	symbol	description	Reset value
31:16	Key	0x5A69 needs to be written at the same time to operate on the other bits of the register	0x0
15:4	-	Reserved	-
3	IRCEN	Internal high-speed oscillation (HSI) enable bit 0: Disable Internal high-speed oscillation 1: Enable internal high-speed oscillation NOTE: The AHB clock source is selected as HSI or when operating Flash, the system automatically enables HSI, independent of this bit.	1
2	-	Reserved	-
1:0	IRCSEL	Internal high-speed oscillation (HSI) frequency select bit 00: 64MHz 01: - 10: - 11: 48MHz Note: When switching different HSI frequencies, it takes about 125us (4 to 5) × T_{LSI} to switch to the selected frequency, during which the CPU is suspended.	0x3

5.3.10 Clock Source Selection Register (CLKSEL)

bit	symbol	description	Reset value
31:16	KEY	The 0x5A69 needs to be written at the same time to operate on the other bits of the register	0x0
15:2	-	Reserved	-
1:0	CLKSEL	AHB clock source select bit 0x0: Internal high-speed oscillation (HSI). 0x1: Write forbidden 0x2: Internal 40KHz low-speed oscillation (LSI). 0x3: Write forbidden Note: Write disable means that the data cannot be written, CLKSEL still selects the previous oscillator	0x0

5.3.11 Clock Source Status Register (CLKSTAT)

bit	symbol	description	Reset value
31:1	-	Reserved	-
0	IRCSTB	Internal high-speed oscillation (HSI) status bits 0: Internal high-speed oscillation is prohibited or unstable 1: Internal high-speed oscillation is stable (HSI is selected by default at power-up) Note: (HSI requires a settling time of about 4 to 6us from off to on). The conditions included are: - The AHB clock is switched from LSI to HSI - The low-power mode switches to HSI operating mode - The system waits for the HSI to stabilize before supplying its clock to the core	1

5.3.12 APB Clock Selection Register (APBCKSEL)

bit	symbol	description	Reset value
31:2	-	Reserved	-
1:0	TMR01SEL	Timer 0/1 clock source select bit 0x0: APBCLK 0x1: forbidden 0x2: forbidden 0x3: forbidden	0x0

5.3.13 IO Multiplexed Status Register (IOMUX)

bit	symbol	description	Reset value
31:12	-	Reserved	-
11:10	RESETPORT	The external reset pin function is read-only 0x3: External reset forbidden 0x2: P10 acts as an external reset port 0x1: P44 acts as an external reset port 0x0: P43 acts as an external reset port	-
9:0	-	Reserved	-

5.3.14 LVD Control Register (LVDCON)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	-	LVD sense voltage selection bit 000: 2.0V 001: 2.2V 010: 2.4V 011: 2.7V 100: 3.0V 101: 3.7V 110: Reserved 111: Reserved Other: Reserved	0x0

5.3.15 P00 Configuration Register (IOP00CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP00CFG	P00 feature selection 0x0: GPIO/AN0 (AN0 function needs to be set to input). 0x1: - 0x2: TXD0 0x3: CTS0 0x4: SPIO_CLK 0x5: CCP0A 0x6: EPWM2 0x7: SWDCLK2 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.16 P01 Configuration Register (IOP01CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP01CFG	P01 feature selection 0x0: GPIO 0x1: AN1 0x2: RXD0 0x3: RTS0 0x4: SPI0_SS 0x5: CCP0B 0x6: EPWM0 0x7: CUSTOM 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.17 P04 Configuration Register (IOP04CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP04CFG	P04 feature selection 0x0: GPIO 0x1: AN2 0x2: - 0x3: CTS1 0x4: SPI0_SS 0x5: CCP0A 0x6: EPWM1 0x7: SPI0_CLK 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.18 P05 Configuration Register (IOP05CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP05CFG	P05 feature selection 0x0: GPIO 0x1: AN3 0x2: - 0x3: RTS1 0x4: SPI0_MOSI 0x5: CCP0B 0x6: EPWM2 0x7: CUSTOM 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.19 P06 Configuration Register (IOP06CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP06CFG	P06 feature selection 0x0: GPIO 0x1: AN4 0x2: - 0x3: SDA0 0x4: SPI0_MISO 0x5: CCP1A 0x6: EPWM3 0x7: CTS1 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.20 P07 Configuration Register (IOP07CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP07CFG	P07 feature selection 0x0: GPIO 0x1: AN5 0x2: - 0x3: SCL0 0x4: SPI0_CLK 0x5: CCP1B 0x6: EPWM4 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.21 P10 Configuration Register (IOP10CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP10CFG	P10 feature selection 0x0: GPIO 0x1: AN6 0x2: TXD0 0x3: - 0x4: - 0x5: CCP0A 0x6: EPWM1 0x7: CTS1 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.22 P12 configuration register (IOP12CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP12CFG	P12 feature selection 0x0: GPIO 0x1: AN7/A1P0 0x2: RXD0 0x3: SDA0 0x4: SPI0_CLK 0x5: CCP1B 0x6: EPWM0 0x7: RTS1 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.23 P13 configuration register (IOP13CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP13CFG	P13 feature selection 0x0: GPIO/ECAP00 0x1: AN8/C0P0 0x2: TXD0 0x3: SCL0 0x4: SPI0_MISO 0x5: CCP1A 0x6: EPWM1 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.24 P14 configuration register (IOP14CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP14CFG	P14 feature selection 0x0: GPIO/ECAP01 0x1: AN9/C0P1 0x2: - 0x3: SDA0 0x4: SPI0_MOSI 0x5: CCP0A 0x6: EPWM4 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.25 P15 configuration register (IOP15CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP15CFG	P15 feature selection 0x0: GPIO/ECAP02 0x1: AN10/C0P2/A1P1 0x2: - 0x3: SCL0 0x4: SPI0_SS 0x5: CCP0A 0x6: EPWM5 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.26 P16 configuration register (IOP16CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP16CFG	P16 feature selection 0x0: GPIO 0x1: - 0x2: RXD0 0x3: SCL0 0x4: CTS0 0x5: CCP0B 0x6: EPWM2 0x7: AN11/OP1_O 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.27 P17 configuration register (IOP17CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP17CFG	P17 feature selection 0x0: GPIO 0x1: AN12/OP1_N 0x2: TXD0 0x3: SDA0 0x4: RTS0 0x5: CCP1A 0x6: EPWM4 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.28 P21 configuration register (IOP21CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP21CFG	P21 feature selection 0x0: GPIO 0x1: AN13/OP1_P 0x2: RXD0 0x3: SCL0 0x4: - 0x5: CCP1B 0x6: EPWM5 0x7: BKIN 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.29 P22 configuration register (IOP22CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP22CFG	P22 feature selection 0x0: GPIO 0x1: AN14 0x2: TXD0 0x3: SCL0 0x4: CTS1 0x5: CCP0A 0x6: EPWM0 0x7: SDA0 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.30 P23 configuration register (IOP23CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP23CFG	P23 feature selection 0x0: GPIO 0x1: AN15/OP0_O 0x2: - 0x3: SDA0 0x4: RTS1 0x5: CCP0B 0x6: EPWM1 0x7: SWDDAT1 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.31 P24 configuration register (IOP24CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP24CFG	P24 feature selection 0x0: GPIO 0x1: AN16/OP0_N 0x2: - 0x3: SDA0 0x4: - 0x5: CCP1A 0x6: EPWM2 0x7: SWDCLK1/3 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.32 P25 configuration register (IOP25CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP25CFG	P25 feature selection 0x0: GPIO 0x1: AN17/OP0_P 0x2: - 0x3: SCL0 0x4: SPI0_SS 0x5: CCP1B 0x6: EPWM3 0x7: C1_O 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.33 P26 configuration register (IOP26CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP26CFG	P26 feature selection 0x0: GPIO 0x1: AN18 0x2: - 0x3: - 0x4: SPI0_CLK 0x5: CCP0A 0x6: EPWM4 0x7: C0_O 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.34 P30 configuration register (IOP30CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP30CFG	P30 feature selection 0x0: GPIO/ECAP13 0x1: AN19/C1P3/A1P2 0x2: RXD0 0x3: - 0x4: SPI0_CLK 0x5: CCP0B 0x6: EPWM0 0x7: CUSTOM 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.35 P31 configuration register (IOP31CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP31CFG	P31 feature selection 0x0: GPIO/ECAP10 0x1: AN20/C1P0/A0P2 0x2: CTS0 0x3: SCL0 0x4: SPI0_MISO 0x5: CCP1A 0x6: EPWM4 0x7: BKIN 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.36 P32 configuration register (IOP32CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP32CFG	P32 feature selection 0x0: GPIO/ECAP11 0x1: AN21/C1P1/A0P1 0x2: RXD0 0x3: SDA0 0x4: SPI0_MOSI 0x5: CCP1B 0x6: EPWM1 0x7: BKIN 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.37 P34 configuration register (IOP34CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP34CFG	P34 feature selection 0x0: GPIO/ECAP12 0x1: AN22/C1P2/A0O 0x2: TXD0 0x3: SDA0 0x4: SPI0_CLK 0x5: CCP0A 0x6: EPWM3 0x7: BKIN 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.38 P35 configuration register (IOP35CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP35CFG	P35 feature selection 0x0: GPIO 0x1: AN23/C1N/A1O 0x2: RTS0 0x3: SCL0 0x4: SPI0_SS 0x5: CCP0B 0x6: EPWM5 0x7: CLKO 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.39 P36 configuration register (IOP36CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP36CFG	P36 feature selection 0x0: GPIO/ECAP03 0x1: AN24/C0P3/A0P0 0x2: - 0x3: - 0x4: CLKO 0x5: CCP1A 0x6: EPWM0 0x7: SWDATA3 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.40 P40 configuration register (IOP40CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP40CFG	P40 feature selection 0x0: GPIO 0x1: AN25 0x2: - 0x3: - 0x4: - 0x5: CCP1B 0x6: EPWM1 0x7: SWDDAT2 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.41 P43 configuration register (IOP43CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP43CFG	P43 feature selection 0x0: GPIO 0x1: AN26/C0N/A0P3 0x2: - 0x3: - 0x4: - 0x5: CCP0A 0x6: EPWM2 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.42 P44 configuration register (IOP44CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP44CFG	P44 feature selection 0x0: GPIO 0x1: AN27/A1P3 0x2: TXD0 0x3: - 0x4: - 0x5: CCP0B 0x6: EPWM1 0x7: - 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.43 P46 configuration register (IOP46CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP46CFG	P46 feature selection 0x0: GPIO 0x1: AN28 0x2: BKIN 0x3: - 0x4: SPI0_MISO 0x5: CCP1A 0x6: EPWM2 0x7: SWDCLK0 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.44 P47 configuration register (IOP47CFG)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3:0	IOP47CFG	P47 feature selection 0x0: GPIO 0x1: AN29 0x2: - 0x3: RTS1 0x4: SPI0_MOSI 0x5: CCP1B 0x6: EPWM5 0x7: SWDDAT0 0x8: TXD1 0x9: RXD1 Other: Reserved	0x0

5.3.45 System Detection Interrupt Enable Register (SYS_IMSC)

bit	symbol	description	Reset value
31:5	-	Reserved	-
4	LVD_IMSC	LVD interrupt enable bit 0: Disable 1: Enable	0x0
3:0	-	Reserved	-

5.3.46 System Detects Interrupt Source Status Registers (SYS_RIS)

bit	symbol	description	Reset value
31:5	-	Reserved	-
4	LVD_RIS	LVD interrupt source state 0: The VDD voltage is higher than the set voltage (no interrupts are generated or the interrupts are cleared). 1: The VDD voltage is lower than the set voltage (generating an interrupt).	0x0
3:0	-	Reserved	-

5.3.47 System Detect Enabled Interrupt Status Registers (SYS_MIS)

bit	symbol	description	Reset value
31:5	-	Reserved	-
4	LVD_MIS	LVD interrupt status 0: No interrupt was generated 1: Enabled and produced an interrupt	0x0
3:0	-	Reserved	-

5.3.48 System Detect Interrupt Clear Register (SYS_ICLR)

bit	symbol	description	Reset value
31:5	-	Reserved	-
4	LVD_ICLR	Write 1 to Clear lvd interrupt status Writing 0 does not affect	0x0
3:0	-	Reserved	-

5.3.49 Internal Oscillation Frequency Trimming Register (HSI_TRIM)

bit	symbol	description	Reset value
31:16	-	0x5A69 needs to be written at the same time to operate on the other bits of the register	0x0
15:8	-	Reserved	-
7:0	TRIM	Internal oscillation frequency adjustment bit When powering up or changing the CLKCON[0] bit, the system automatically loads the factory trimming value	-

5.3.50 SRAM write enable register (SRAMLOCK)

bit	symbol	description	Reset value
31:16	LOCK	When LOCK=0x55AA, the protection function of SRAM takes effect	0x0
15:4	-	Reserved	-
3:0	REGION	Bit3: Set the SRAM address 0x20001800-0x20001FFF area to a write-protected state Bit2: Set the SRAM address 0x20001000-0x200017FF area to write-protected Bit1: Set the SRAM address 0x20000800-0x20000FFF area to write-protected Bit0: - Write 0 protection function disabled (R/W) Write 1 protection function is enabled (only reads allowed) Note: The 2KBytes area with an initial address range of 0x20000000-0x2000 07FF is free to read and write.	0x0

5.3.51 GPIO0 write enable register (GPIO0LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables GPIO0 related register to read the value of 0x99 When LOCK= other values, operation of the GPIO0-related registers is prohibited	0x0

5.3.52 GPIO1 write enable register (GPIO1LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables GPIO1 related register to read the value of 0x99 When LOCK= other values, operation of the GPIO1-related registers is prohibited	0x0

5.3.53 GPIO2 write enable register (GPIO2LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables the GPIO2 related register to read the value 0x99 When LOCK= other values, operation of GPIO2-related registers is prohibited	0x0

5.3.54 GPIO3 write enable register (GPIO3LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables the GPIO3-related registers to be read as 0x99 When LOCK= other values, operation of GPIO3-related registers is prohibited	0x0

5.3.55 GPIO4 write enable register (GPIO4LOCK)

bit	symbol	description	Reset value
31:0	LOCK	When LOCK=0x99, enables the operation of the GPIO4-related registers and reads a value of 0x99 When LOCK=other values, operation of GPIO4-related registers is prohibited	0x0

5.3.56 The port configuration write enable register (IOCFGLOCK)

bit	symbol	description	Reset value
31:0	IOCFGLOCK	When LOCK=0x99, enables the operation port to configure the related registers and reads a value of 0x99 When LOCK=other values, disable the operation port to configure the associated registers	0x0

6. System Timer (SysTick)

The Cortex-M0® has a built-in system timer, SysTick, which provides a simple 24-bit write clear, decrement counting, auto-loading of initial values, and registers with flexible control mechanisms. The counter can be used as a tick timer for a real-time operating system (RTOS) or as a simple timer peripheral.

When the system timer is enabled, the value of the SysTick current value register (SysTickVAL) is counted down to 0, and at the next clock edge, the value of the SysTick reload value register (SysTickLOAD) is reloaded, and then decremented at any time. When the counter is decremented to 0, the COUNTFLAG status bit is set to 1 and the SysTickCTRL register is read to clear the COUNTFLAG bit.

The clock source for the system timer is the system clock (SCLK).

NOTE: When the kernel is in a suspended state, the count stops decrementing.

6.1 Register mapping

(SysTick base address = 0xE000_E010) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
SysTickCTRL	0x000	R/W	SysTick control and status register	0x0
SysTickLOAD	0x004	R/W	SysTick reloads value register	-
SysTickVAL	0x008	R/W	SysTick current value register	-
SysTickCALIB	0x00C	RO	SysTick calibration value register	0x40028B0A

6.2 Register description

6.2.1 SysTick Control and Status Register (SysTickCTRL)

bit	symbol	description	Reset value
31:17	-	Reserved	-
16	COUNTFLAG	When the SysTick counter decrements the count to 0, the bit is set, read the register will clear the bit.	0x0
15:2	-	Reserved	-
1	INT	SysTick interrupt enable bit 0: Disable SysTick Interrupt 1: Enable SysTick interrupt	0x0
0	IN	The SysTick counter enables bits 0: Disable 1: Enable	0x0

6.2.2 SysTick reload register (SysTickLOAD)

bit	symbol	description	Reset value
31:24	-	Reserved	-
23:0	RELOAD	When the counter is enabled and counted to 0, this value reloads the SysTickVAL register.	-

6.2.3 SysTick current value register (SysTickVAL)

bit	symbol	description	Reset value
31:24	-	Reserved	-
23:0	CURRENT	The current value of the SysTick counter is returned when the register is read; Write any data to clear the SysTick counter while clearing the COUNTFLAG bit in the SysTickCTRL register.	-

6.2.4 SysTick calibration value register (SysTickCALIB)

bit	symbol	description	Reset value
31	-	Reserved	-
30	SKEW	Shows whether TENMS value is accurate, an inaccurate TENMS value will affect the match of SysTick as a software real-time clock. 0: The values of TENMS are accurate; 1: The value of TENMS is inaccurate or does not exist.	0x0
29:24	-	Reserved	-
23:0	TENMS	It is a reloaded value for 10ms timing and is affected by the system clock deviation. If this value is read as 0, the calibration value is indeterminate.	0x000004

7. Nested Vector Interrupt Controller (NVIC)

The Cortex-M0® CPU provides a nested vector interrupt controller (NVIC) for interrupt handling.

7.1 characteristic

- Nested vector interrupts are supported.
- Automatically save and restore processor state.
- Dynamically change priorities.
- Simplify and determine interrupt times.

NVIC handles all supported exceptions in priority. All exceptions are handled in "Handler mode". The NVIC supports 32 (IRQ[31:0]) discrete interrupts, each with 4 levels of interrupt priority. All Interrupts and most system exceptions can be configured with different priorities. When an interrupt occurs, NVIC will prioritize the new interrupt against the current interrupt, and if the new interrupt has a high priority, the new interrupt will be processed immediately.

When an interrupt is accepted, the start address of the interrupt service program (ISR) is available from the in-memory vector table. The software does not need to decide which interrupt is responded to, nor does it need to assign the start address of the relevant ISR. When the start address is obtained, the NVIC automatically saves the processor status registers (PC, PSR, LR, R0~R3, R12) to the stack. After the ISR ends, the NVIC will recover the values of the relevant registers from the stack and run in a normal state. So it takes a small and certain amount of time to process the interrupt request.

NVIC supports "end-to-end chaining" that can effectively handle back-to-back interrupts, i.e. without saving and restoring the current state, thereby reducing the delay in completing the current ISR to switching to a pending ISR. NVIC also supports "Late Arrival", so it can improve the efficiency of concurrent interrupts. When a higher priority interrupt request occurs before the current ISR starts executing (the stage of saving the processor state and getting the start address), NVIC will immediately process the higher priority interrupt, improving real-time.

For more details, please refer to the ARM®Cortex-M0® Technical Reference Manual and the ARM®v6-M Architecture Reference Manual.

7.2 Exception patterns and system interrupt mapping

The following table lists the exception patterns supported by the series. As with all interrupts, the software can set a level 4 priority for some of these exceptions. The highest user-configurable priority is 0 and the lowest priority is 3. The default priority for all user-configurable interrupts is 0.

Exception name	Exception number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4~10	Reserved
SVCall	11	Configurable
Reserved	12~13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0~IRQ31)	16~47	Configurable

Note: Priority 0 is the 4th priority in the system, after the three system exceptions of "Reset", "NMI", and "Hard Fault".

7.3 Vector table

Exception number	Interrupt	Vector address	The exception type	description
1-15	-	0x00-0x3c	System exception	-
16	0	0x40	GPIO0	P0[7:0] Interrupt
17	1	0x44	GPIO1	P1 [7:0] interrupt
18	2	0x48	GPIO2	P2 [7:0] interrupt
19	3	0x4c	GPIO3	P3 [7:0] interrupt
20	4	0x50	GPIO4	P4 [7:0] interrupt
21	5	0x54	-	-
22	6	0x58	CCP	Capture/PWM interrupt
23	7	0x5c	ADC0	ADC0 interrupt
24	8	0x60	-	-
25	9	0x64	WWDT	WWDT interrupt
26	10	0x68	EPWM	EPWM interrupt
27	11	0x6c	-	-
28	12	0x70	ADC1	ADC1 interrupt
29	13	0x74	ACMP	ACMP interrupt
30	14	0x78	-	
31	15	0x7c	UART0	UART0 interrupt
32	16	0x80	UART1	UART1 interrupt
33	17	0x84	-	-
34	18	0x88	-	-
35	19	0x8c	TIMER0	Timer0 interrupt
36	20	0x90	TIMER1	Timer1 interrupt
37	21	0x94	-	-
38	22	0x98	-	-
39	23	0x9c	WDT	Watchdog interrupt
40	24	0xa0	I2C	I2C interrupt
41	25	0xa4	-	-
42	26	0xa8	SSP/SPI	SSP/SPI interrupt
43	27	0xac	-	-
44	28	0xb0	-	-
45	29	0xb4	-	-
46	30	0xb8	-	-
47	31	0xbc	SYS_CHK	system detect interrupt (LVD interrupt).

7.4 Register mapping

(NVIC Base Address = 0xE000_E000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
ISER	0x100	R/W	interrupt set enable control register	0x0
ICER	0x180	R/W	Interrupt clear enable control register	0x0
ISPR	0x200	R/W	Interrupt set pending control register	0x0
ICPR	0x280	R/W	Interrupt clear pending control register	0x0
IPR0	0x400	R/W	IRQ0~IRQ3 interrupt priority register	0x0
IPR1	0x404	R/W	IRQ4~IRQ7 interrupt priority register	0x0
IPR2	0x408	R/W	IRQ8~IRQ11 interrupt priority register	0x0
IPR3	0x40C	R/W	IRQ12~IRQ15 interrupt priority register	0x0
IPR4	0x410	R/W	IRQ16~IRQ19 interrupt priority register	0x0
IPR5	0x414	R/W	IRQ20~IRQ23 interrupt priority register	0x0
IPR6	0x418	R/W	IRQ24~IRQ27 interrupt priority register	0x0
IPR7	0x41C	R/W	IRQ28~IRQ31 interrupt priority register	0x0

7.5 Register description

7.5.1 Interrupt set enable control register (ISER)

bit	symbol	description	Reset value
31:0	SEVENTH	Interrupt enable bit Enables one or more interrupts. Each bit represents an interrupt from IRQ0 to IRQ31 (Vector number from 16 to 47). Write operation: 0: invalid 1: Write 1 to enable the relevant interrupt Read action: 0: The relevant interrupt status is prohibited 1: The relevant interrupt state is enabled NOTE: Reading the register value indicates the current enable state.	0x0

7.5.2 Interrupt Clear Enable Control Register (ICER)

bit	symbol	description	Reset value
31:0	CLRENA	Interrupt disable bit Disable one or more interrupts. Each bit represents an interrupt from IRQ0 to IRQ31 (Vector number from 16 to 47). Write operation: 0: invalid 1: Write 1 to disable related interrupts Read action: 0: The relevant interrupt status is prohibited 1: The relevant interrupt state is enabled NOTE: Reading the register value indicates the current enable state.	0x0

7.5.3 Interrupt set pending Control Register (ISPR)

bit	symbol	description	Reset value
31:0	SETPEND	Sets the interrupt pending bit Write operation: 0: invalid 1: Write 1 to set the pending state. Each bit represents an interrupt from IRQ0 to IRQ31 (vector number from 16 to 47). Read operation: 0: The related interrupt is not in the pending state 1: The related interrupt is in a pending state NOTE: Reading the register value indicates the current pending state.	0x0

7.5.4 Interrupt Clean pending Control Register (ICPR)

bit	symbol	description	Reset value
31:0	CLRPEND	Clear the interrupt pending bit Write operation: 0: invalid 1: Write 1 to clear the pending state. Each bit represents an interrupt from IRQ0 to IRQ31 (vector number from 16 to 47). Read action: 0: The related interrupt is not in the pending state 1: The related interrupt is in a pending state Note: Reading the register value indicates the current pending state.	0x0

7.5.5 IRQ0~IRQ3 interrupt priority register (IPR0)

bit	symbol	description	Reset value
31:30	PRI_3	IRQ3 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_2	IRQ2 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_1	IRQ1 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_0	IRQ0 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

7.5.6 IRQ4~IRQ7 interrupt priority register (IPR1)

bit	symbol	description	Reset value
31:30	PRI_7	IRQ7 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_6	IRQ6 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_5	IRQ5 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_4	IRQ4 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

7.5.7 IRQ8~IRQ11 interrupt priority register (IPR2)

bit	symbol	description	Reset value
31:30	PRI_11	IRQ11 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_10	IRQ10 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_9	IRQ9 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_8	IRQ8 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

7.5.8 IRQ12~IRQ15 interrupt priority register (IPR3)

bit	symbol	description	Reset value
31:30	PRI_15	IRQ15 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_14	IRQ14 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_13	IRQ13 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_12	IRQ12 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

7.5.9 IRQ16~IRQ19 Interrupt Priority Register (IPR4)

bit	symbol	description	Reset value
31:30	PRI_19	IRQ19 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_18	IRQ18 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_17	IRQ17 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_16	IRQ16 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

7.5.10 IRQ20~IRQ23 interrupt priority register (IPR5)

bit	symbol	description	Reset value
31:30	PRI_23	IRQ23 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_22	IRQ22 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_21	IRQ21 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_20	IRQ20 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

7.5.11 IRQ24~IRQ27 interrupt priority register (IPR6)

bit	symbol	description	Reset value
31:30	PRI_27	IRQ27 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_26	IRQ26 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_25	IRQ25 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_24	IRQ24 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

7.5.12 IRQ28~IRQ31 interrupt priority register (IPR7)

bit	symbol	description	Reset value
31:30	PRI_31	IRQ31 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_30	IRQ30 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
21:16	-	Reserved	-
15:14	PRI_29	IRQ29 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
13:8	-	Reserved	-
7:6	PRI_28	IRQ28 priority 0 indicates the highest priority and 3 indicates the lowest priority	0x0
5:0	-	Reserved	-

8. System Control Module (SCB)

The Status and Operating Mode of the Cortex-M0® are managed by the System Control Module. The associated registers of these system control modules allow you to control CPUID, Cortex-M0® interrupt priority, and Cortex-M0® power management.

For more details, please refer to the "ARM®Cortex-M0® Technical Reference Manual" and the "ARM®v6-M Architecture Reference Manual" 。

8.1 Register mapping

(SCB base address = 0xE000_ED00). RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
CPUID	0x000	RO	CPUID register	0x410CC200
ICSR	0x004	R/W	Interrupt control status register	0x0
AIRCR	0x00C	R/W	Apply interrupt and reset control registers	0xFA050000
SCR	0x010	R/W	System control registers	0x0
SHPR2	0x01C	R/W	System processor priority register 2	0x0
SHPR3	0x020	R/W	System processor priority register 3	0x0

8.2 Register description

8.2.1 CPUID register (CPUID)

bit	symbol	description	Reset value
31:24	Implementer	Implement the code = 0x41, assigned by ARM	0x41
23:20	Variant	The version number 0x0	0x0
19:16	Constant	Processor architecture = 0xC, which represents the ARMv6-M architecture	0xC
15:4	Partno	Processor product number =0xC20, which stands for Cortex-M0	0xC20
3:0	Revision	Revision number 0x0	0x0

8.2.2 Interrupt Control Status Register (ICSR)

bit	symbol	description	Reset value
31	NMIPENDSET	The NMI sets the pending bit Write operation: 0= invalid 1= set the NMI exception as pending Read operation: 0= The NMI exception is not pending 1= NMI exception is pending Note: Since NMI is the highest priority exception, the processor usually enters NMI exception handling as soon as it detects the bit write 1. After exception handling is entered, the processor clears out the bit. This means that only when the processor is executing the NMI exception handler, the NMI signal is generated again, and the NMI exception handler reads this bit and returns 1.	0x0
30:29	-	Reserved	-
28	PENDSVSET	PendSV sets the pending bit Write operation: 0= invalid 1= Set the PendSV exception as pending Read operation: 0= The PendSV exception is not pending 1= PendSV exception is pending Note: Setting this bit to 1 is the only way to set pending PendSV exceptions.	0x0
27	PENDSVCLR	PendSV clears the pending bit Write operation: 0= invalid 1= Clears the PendSV exception pending state Note: This bit is a write-only bit. In order to clear the PENDSV bit, you must write 0 to PENDSVSET and 1 to PENDSVCLR at the same time.	-
26	PENDSTSET	The SysTick exception sets the pending bit Write operation: 0= invalid 1= Set the SysTick exception Pending Read operation: 0= The SysTick exception is not pending 1= SysTick exception is pending	0x0
25	PENDSTCLR	SysTick exception clears the pending bit Write operation: 0= invalid 1= Clears the SysTick exception pending state Note: This bit is read-only. When you want to clear the PENDST bit, you must write 0 to PENDSTSET and 1 to PENDSTCLR at the same time.	-
24	-	Reserved	-
23	ISRPREEMPT	Interrupt preemptive occupied bit If this bit set to 1, a pending exception exits from the debug stop state and enters exception handling. Note: This bit is read-only	-
22	ISRPENDING	Interrupt pending flag (excluding NMI and Faults) 0= The interrupt is not pending 1= Interrupt is pending	0x0

		NOTE: This bit is read-only	
21	-	Reserved	-
20:12	VECTPENDING	The highest priority exception number among pending exceptions 0= There are no exceptions pending Non-0= The highest priority exception number among pending exceptions Note: These bits are read-only	0x0
11:9	-	Reserved	-
8:0	VECTACTIVE	Contains the current execution exception number 0= Thread mode Non-0= The exception number of the current executing exception Note: These bits are read-only	0x0

8.2.3 Apply interrupt and reset control registers (AIRCR)

bit	symbol	description	Reset value
31:16	VECTORKEY	Register access key Write operation: - When writing this register, the VECTORKEY bit field must be set to 0x05FA, otherwise writes will be ignored. - The VECTORKEY bit field is used to prevent the register from being written incorrectly when the system resets or clears the abnormal state. Read operation: The value read out is 0xFA05	0xFA05
15	ENDIANESS	The endianess format of the memory read only 0= Little-endian 1= main aspects	0x0
14:3	-	Reserved	-
2	SYSRESETREQ	System reset request Writing 1 to this bit will cause a reset signal to the chip, indicating that there is a reset request. This bit is a write-only bit, and it is automatically cleared to zero after reset.	0x0
1	VECTCLRACTIVE	Abnormally valid status clear bit Reserved for debugging use. When writing this register, the user must write 0 to that bit, otherwise unpredictable situations will occur.	0x0
0	-	Reserved	-

8.2.4 System Control Register (SCR)

bit	symbol	description	Reset value
31:5	-	Reserved	-
4	SEVONPEND	Sends an event when pending 0= Only enable interrupts or events can wake up the processor, excluding disabled interrupts. 1= Enable events and all interrupts, including disabled interrupts, to wake up the processor. When an event or interrupt enters a pending state, the event signal wakes the processor from the WFE. If the processor is not waiting for an event, the event will be registered and affect the next WFE. Executing SEV instructions or external events also wakes up the processor.	0x0
3	-	Reserved	-
2	SLEEPDEEP	Processor deep sleep and sleep mode selection Controls whether the processor uses sleep mode in low-power mode or deep sleep mode. 0= Sleep mode 1= Deep sleep mode	0x0
1	SLEEPONEXIT	Sleep-On-Exit enabled This bit indicates whether to exit sleep when returning to Thread mode from Handler mode 0= When returned from Thread mode, it does not hibernate 1= When returning to Thread mode from the ISR, go into hibernation or deep hibernation This bit set to 1 enables an interrupt-driven application, thus avoiding returning to an empty main function application.	0x0
0	-	Reserved	-

8.2.5 System Processor Priority Register 2 (SHPR2)

bit	symbol	description	Reset value
31:30	PRI_11	System Exception Number 11 – Priority of SVCall 0: Highest priority 3: Indicates the lowest priority	0x0
29:0	-	Reserved	-

8.2.6 System Processor Priority Register 3 (SHPR3)

bit	symbol	description	Reset value
31:30	PRI_15	System exception number 15 – Priority of SysTick 0: Highest priority 3: Indicates the lowest priority	0x0
29:24	-	Reserved	-
23:22	PRI_14	System exception number 14 – Priority of PendSV 0: Highest priority 3: Indicates the lowest priority	0x0
21:0	-	Reserved	-

9. General Purpose I/O (GPIO)

9.1 overview

Up to 24 general-purpose I/O pins, each I/O port can be configured by software into a normal input, pull-up input, pull-down input, push-pull output, and no pull-out leakage output mode. These pins can be shared by configuring the chip and other functional pins.

9.2 characteristic

- Five I/O modes.
  - Normal input.
  - Pull-up input.
  - Pull-down input.
  - Push-pull output.
  - Open-drain output without pull-up.
- I/O can be configured to trigger interrupts at edges/levels.
- 2 output current configurations.
- 2-stage I/O speed configuration.

9.3 Feature description

9.3.1 Input mode

Set GPIOxPMS [4n+2:4n] to 000, Px.n pins to input mode, I/O pins to high-impedance state, no drive capability.

9.3.2 Pull-up input mode

Set GPIOxPMS [4n+2:4n] to 001, Px.n pins to pull-up input mode, and I/O pins to internally connect pull-up resistors.

9.3.3 Pull-down input mode

Set GPIOxPMS [4n+2:4n] to 100, Px.n pins to pull-down input mode, and I/O pins to internally connect pull-down resistors.

9.3.4 Push-pull output mode

Set GPIOxPMS [4n+2:4n] to 001, Px.n pins to push-pull output mode, and I/O support digital output function with source/sink current capability. The value of the DO corresponding bit[n] is sent to the corresponding pin.

9.3.5 Open-drain output without pull-up

Set GPIOxPMS [4n+2:4n] to 010, Px.n pins to open-drain output mode, I/O pin digital output function only supports current sinking, and pull resistors are required to drive high. If the DO corresponding bit is '0', the output is low on the pins. If the DO corresponding bit is '1', the pin is set high by an external pull-up resistor.

9.3.6 Interrupt and wake-up capabilities

Each GPIO pin can be set as an interrupt source for the chip. There are five interrupt trigger conditions that can be set: low trigger, high trigger, falling edge trigger, rising edge trigger, and rising and falling edge triggering at the same time. In edge triggering, the user can prevent unexpected interrupts caused by noise by enabling the input signal debounce function.

When the chip enters sleep/deep sleep/stop mode, the GPIO can also wake up the system. The conditions triggered by wake-up are determined by GPIOxIVAL and require the following attention:

The falling edge wakes up needs to raise the port level before entering a low-power state.

The rising edge wakes up requires the port level to be pulled low before entering a low-power state.

9.4 Register mapping

GPIO0 base address = 0x5200_0000;

GPIO1 base address = 0x5280_0000;

GPIO2 base address = 0x5300_0000;

GPIO3 base address = 0x5380_0000;

GPIO4 base address = 0x5400_0000;

RO: read-only; WO: Write only; R/W: Read and write. The x values in the following registers range from 0-5.

register	Offset	R/W	description	Reset value
PMS(P1A)	0x000	R/W	GPIOx mode select register	0x0
DOM(P1A)	0x004	R/W	GPIOx data output write mask registers	0x0
DO(P1A)	0x008	R/W	GPIOx data output register	0xff
OF	0x00c	RO	GPIOx pin status data register	-
IMSC(P1A)	0x010	R/W	GPIOx interrupt enable register	0x0
RICE	0x014	RO	GPIOx interrupt source status register	0x0
PUT	0x018	RO	GPIOx enabled interrupt status registers	0x0
ICLR(P1A)	0x01c	WO	GPIOx interrupt state clear register	0x0
ITYPE(P1A)	0x020	R/W	GPIOx interrupt trigger mode register	0x0
IVAL(P1A)	0x024	R/W	GPIOx interrupt trigger value register	0x0
IANY(P1A)	0x028	R/W	GPIOx interrupt edge trigger mode	0x0
DIDB(P1A)	0x02c	R/W	GPIOx input filtering control register	0x0
DOSET(P1A)	0x030	WO	GPIOx output set register	0x0
DOCLR(P1A)	0x034	WO	GPIOx output clear register	0x0
DR(P1A)	0x038	R/W	GPIOx drive current set register	0xff
SR(P1A)	0x03C	R/W	GPIOx output rate setting register	0xff

Note:

1) (P1A) The registers marked are protected registers.
2) (P1A): When GPIOxLOCK=99H, the marked register is allowed to write; = Other values, forbidden to write.
3) GPIOxLOCK registers are shown in the system control section.

9.5 Register description

9.5.1 GPIOx Mode Selection Register (GPIOxPMS)

bit	symbol	description	Reset value
31	-	Reserved	-
30:28	PMS7	Px.7 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: Reserved	0x0
27	-	Reserved	-
26:24	PMS6	Px.6 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: Reserved	0x0
23	-	Reserved	-
22:20	PMS5	Px.5 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: Reserved	0x0
19	-	Reserved	-
18:16	PMS4	Px. 4 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: Reserved	0x0
15	-	Reserved	-
14:12	PMS3	Px. 3 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: Reserved	0x0
11	-	Reserved	-
10:8	PMS2	Px.2 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up	0x0

		0x3: Pull-up input 0x4: Pull-down input Other values: Reserved	
7	-	Reserved	-
6:4	PMS1	Px.1 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: Reserved	0x0
3	-	Reserved	-
2:0	PMS0	Px.0 mode selection 0x0: Normal input 0x1: Push-pull output 0x2: Open-drain output without pull-up 0x3: Pull-up input 0x4: Pull-down input Other values: Reserved	0x0

9.5.2 GPIOx data output write mask register (GPIOxDOM)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	HOUSE	Px[7:0] The data output write mask bit 1: DO register This bit of data is not writable 0: DO registers this bit of data is writable	0x0

9.5.3 GPIOx Data Output Register (GPIOxDO)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	DO'S	Px[7:0] output value 1: Output high 0: Output low	0xFF

9.5.4 GPIOx Pin Status Register (GPIOxDI)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	OF	Pin status input data	-

9.5.5 GPIOx interrupt enable register (GPIOxIMSC)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	IMSC	Px [7:0] interrupt enable bit 1: Enable 0: Disable	0x0

9.5.6 GPIOx interrupt source status register (GPIOxRIS)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	RICE	Px[7:0] interrupt source status bit 1: The pins caused a break 0: The pins are not interrupted	0x0

9.5.7 GPIOx enabled interrupt status register (GPIOxMIS)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	PUT	Px[7:0] enabled interrupt status bit 1: A pin interrupt is enabled and an interrupt is generated 0: No interrupt was generated	0x0

9.5.8 GPIOx interrupt state clear register (GPIOxICLR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	ICLR	Px[7:0] Interrupt state clears zero Write 1 and zero out the corresponding bits of GPIOxRIS and GPIOxMIS	0x0

9.5.9 GPIOx interrupt trigger mode selection register (GPIOxITYPE)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	ITYPE	Px [7:0] Interrupt trigger mode select bit 0: Edge triggering 1: Level triggering	0x0

9.5.10 GPIOx interrupt trigger value register (GPIOxIVAL)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	IVAL	Px[7:0] Interrupt/Sleep Wake Trigger Condition Selection Bit 0: Low-level triggering or falling edge triggering 1: High-level triggering or rising edge triggering	0x0

9.5.11 GPIOx interrupt edge trigger mode register (GPIOxIANY)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	IANY	Px[7:0] Interrupt edge trigger mode select bit 0: The falling or rising edge is triggered, determined by the GPIOxIVAL register 1: Both the rising and falling edges can be triggered	0x0

9.5.12 GPIOx Input Filter Control Register (GPIOxDIDB)

bit	symbol	description	Reset value
31:10	-	Reserved	-
9:8	DBCKS	Px input filtering sampling clock selection bits 000: HCLK 001: HCLK/2 010: HCLK/4 011: HCLK/6 100: HCLK/8 101: HCLK/10 110: HCLK/12 111: HCLK/14	0x0
7:0	DIDB	Px[7:0] Input filter enable bit 0: The pin level is detected via the Smit input directly to GPIOxDI and the interrupt edge 1: After the pin level passes through the Smit input, it also needs to be filtered to GPIOxDI and interrupt edge detection Note: The filter circuit consists of a 3-stage DFF and a debounce circuit that filters out positive/negative pulses with input single pulse widths less than two filtered sample clocks. (Filterable pulse width range: .) 42ns~580ns@Fsys=48MHz)	0x0

9.5.13 GPIOx output position register (GPIOxDOSET)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	OF	Px[7:0] Output set control bit writes: 0= Does not affect 1= GPIOxDO corresponds to a high bit output (The register is a write-only register and reads as an invalid value)	0x0

9.5.14 GPIOx output clear register (GPIOxDOCLR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	DOC	Px[7:0] Output Zero Control Bit Write: 0= Does not affect 1= GPIOxDO corresponds to a low bit output (The register is a write-only register and reads as an invalid value)	0x0

9.5.15 GPIOx Drives Current Set Register (GPIOxDR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	DR	Px [7:0] drive current set bit 0= Large drive current 1= Small drive current	0xff

9.5.16 GPIOx output rate setting register (GPIOxSR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	SR	Px[7:0] output rate setting bit 0= The output rate is fast 1= The output rate is slow	0xff

10. Watchdog Timer (WDT)

10.1 overview

The watchdog timer is designed to reset the system when it is running to an unknown state. This approach prevents the system from entering an indefinite cycle. In addition, the watchdog timer supports the system wake-up function from sleep/deep sleep mode.

10.2 characteristic

- 32-bit free downward counter.
- WDT_CLK=40KHz。
- Support WDT interrupt and WDT reset function.
- It has WDT register write protection to avoid abnormal operation.

10.3 Feature description

WDT can be set in the user configuration to start after power-on reset of the WDT counter and WDT overflow reset enable (WDTEN=00H after reset), which requires the user configuration bit CONFIG_EN_WDT to be enabled.

After the system reset is complete, WDTLOAD loads the data in the user configuration WDT_TIME, that is, the WDTLOAD default is determined by the WDT_TIME. The WDT overflow time defined by the user can not be defined by the WDT_TIME by modifying the value of the WDTLOAD.

The overflow time is calculated as: $T_{WDTOVER}$=WDTLOAD× count clock period (select the watchdog clock via WDTCON [3:2]).

If the CONFIG_EN_WDT is set to Disabled, the power-on reset of the WDT counter defaults to the stop count state, and there are 2 ways to make the WDT counter start counting after the reset is completed:

1) WDTEN (WDT Reset Enable Control Bit) writes a value that is not equal to 5AH.
2) WDTIEN (WDT Interrupt Enable Control Bit) Write 1.

If the system has a WDT reset, the power-on configuration process is re-performed after the WDT reset, and the reset time is about 4.5ms. After the reset, the WDT count is started and then the WDT reset is started, the time is determined by the WDTLOAD. The interval between the two resets is about 4.5 ms+2×$T_{WDTOVER}$.

After the WDT starts the counter, the 32-bit counter starts at the initial value and counts down, when the count reaches 0, a WDT interrupt is generated, the initial value is automatically loaded, and the downward count is re-counted, and when the second interrupt is generated and the last interrupt flag bit is not cleared, a WDT reset is generated (required).

10.4 Register mapping

(WDT base address = 0x4780_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
CON(P1D)	0x000	R/W	WDT control registers	0x5A00
LOAD(P1D)	0x004	R/W	WDT initial value register	-
VAL	0x008	RO	WDT count value	0xFFFFFFFF
RICE	0x00c	RO	WDT interrupt source status register	0x0
PUT	0x010	RO	WDT enabled interrupt status register	0x0
ICLR(P1D)	0x014	WO	WDT interrupt clear register	-
LOCK	0x500	R/W	WDT write-protect registers	0x0

Note: 1) (P1D) The registers marked are protected registers.

2） (P1D): When LOCK=55AA6699H, the marked register is allowed to write; = Other values, forbidden to write.

10.5 Register description

10.5.1 WDT Control Register (WDTCON)

bit	symbol	description	Reset value
31:17	-	Reserved	-
16	DEBUG	DEBUG mode control 0: WDT stop count when the simulation state is paused 1: The WDT count is independent of the simulation state	0x0
15:8	WDTEN	WDT reset enable 0x5A: Disable WDT reset Other values: Enables WDT reset, when there is no clear interrupt flag after a WDT interrupt occurs, trigger a WDT reset is triggered the next time a WDT interrupt occurs. When enabled reset, whether WDTCON[0] is 1 or not, the WDT interrupt is enabled	0x5A
7:4	-	Reserved	-
3:2	WDTPRE	WDT clock selection 0x0: WDT_CLK/1 0x1: WDT_CLK/16 0x2: WDT_CLK/256 0x3: Reserved	0x0
1	-	Reserved	-
0	WDTIEN	WDT interrupt enablement 0: Disables WDT Interrupts 1: Enables WDT interrupts	0x0

10.5.2 WDT Initial Register (WDTLOAD)

bit	symbol	description	Reset value
31:0	WDTLOAD	The WDT counts the initial value. The minimum value is 1	-

10.5.3 WDT count value (WDTVAL)

bit	symbol	description	Reset value
31:0	WDTVAL	The current value of the WDT counter	0xFFFFFFFF

10.5.4 WDT interrupt source status register (WDTRIS)

bit	symbol	description	Reset value
31:1	-	Reserved	-
0	WDTRIS	1: Produces a WDT count down overflow interrupt 0: No interrupt was generated	0x0

10.5.5 WDT enabled Interrupt Status Register (WDTMIS)

bit	symbol	description	Reset value
31:1	-	Reserved	-
0	WDTMIS	1: Enables a WDT interrupt and produces an interrupt 0: No interrupt was generated	0x0

10.5.6 WDT Interrupt clear Register (WDTICLR)

bit	symbol	description	Reset value
31:0	WDTICLR	write 0x55AA55AA: Clear the interrupt flag bit and reload the initial value Other values: Does not affect	-

10.5.7 WDT Write Protection Register (WDTLOCK)

bit	symbol	description	Reset value
31:0	WDTREN	write 0x55AA6699: Enables the operation of the WDT-related registers, which read as 0x01 Other values: Disable the operation of WDT-related registers and read as 0x00	0x0

11. Window Watchdog Timer (WWDT)

11.1 overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specific window time to prevent the program from running into an uncontrollable state under unpredictable conditions.

11.2 characteristic

- The 6-bit down-count value (CNTDAT) and the 6-bit window comparison value (CMPDAT) make the window period more flexible.
- Supports 4-bit value (PSCSEL) selection window watchdog prescale value, and the prescale counter can reach up to 14 bits.

11.3 Feature description

When WWDT is enabled, the 6-bit counter counts down starting from 0x3F, which triggers a WWDT reset:

1) Performs a reload operation when WWDTVAL > CMPDAT.
2) When the WWDTVAL is reduced to 0x00.

Time to overflow when the WWDT counter counts from 0x3F to 0: (PSCSEL×1024×64) × T_{APBCLK}.

The reload operation can only be performed when CMPDAT>=WWDTVAL>0 will not cause a WWDT reset. When an interrupt is enabled, WWDTVAL=CMPDAT generates an interrupt (it is recommended to perform a reload operation in the interrupt service program before clearing the interrupt flag).

11.4 Register mapping

(WWDT base address = 0x4180_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
WITH	0x000	R/W	WWDT control registers	0x80000000
RL	0x004	WO	WWDT overload register	-
VAL	0x008	RO	WWDT count value	0x3F
RICE	0x00c	RO	WWDT interrupt source status register	0x0
PUT	0x010	RO	The WWDT enabled Interrupt status register	0x0
ICLR	0x014	WO	WWDT interrupt clear register	-

11.5 Register description

11.5.1 WWDT Control Register (WWDTCON)

bit	symbol	description	Reset value
31	DEBUG	0: When the simulation state is paused, the WWDT count is not affected 1: When the simulation state is paused, the WWDT count is paused	1
30:22	-	Reserved	-
21:16	CMPDAT	Window comparison values	0x00
15:8	-	Reserved	-
7:4	PSCSEL	0000: Divide-by-2 0001: Divide-by-4 0010: Divide-by-8 0011: Divide-by-16 0100: Divide by 32 0101: Divide by 64 0110: Divide by 128 0111: Divide by 256 1000: Divide by 512 1001: Divide-by-1024 1010: Divide-by-2048 1011: Divide-by-4096 1100: Divide-by-8192 1101: Divide-by-16384 1110: Divide-by-16384 1111: Divide-by-16384	0x0
3	-	Reserved	-
2	WWDTRF	0: No WWDT reset occurred 1: A WWDT reset occurred	0x0
1	WWDTIEN	WWDT interrupt enable 0: Disables WWDT Interrupt 1: Enables WWDT interrupt	0x0
0	WWDTEN	WWDT enable 0: WWDT modules are disabled 1: Enables the WWDT module	0x0

11.5.2 WWDT Overload Register (WWDTRL)

bit	symbol	description	Reset value
31:0	WWDTRL	Write 0x55AA, reload the WWDT count value to 0x3F	-

11.5.3 WWDT Count Value (WWDTVAL)

bit	symbol	description	Reset value
31:6	-	-	-
5:0	WDTVAL	The current value of the WDT counter	0x3F

11.5.4 WWDT interrupt source status register (WWDTRIS)

bit	symbol	description	Reset value
31:1	-	Reserved	-
0	WWDTRIS	1: a WWDT matching interrupt generated 0: No interrupt was generated	0x0

11.5.5 WWDT enabled Interrupt status register (WWDTMIS)

bit	symbol	description	Reset value
31:1	-	Reserved	-
0	WWDTMIS	1: Enables WWDT interrupt and produced an interrupt 0: No interrupt was generated	0x0

11.5.6 WWDT interrupt clear register (WWDTICLR)

bit	symbol	description	Reset value
31:1	-	Reserved	-
0	WDTICLR	Write 1 to clear the interrupt flag bit Other values: Does not affect	-

12. Cyclic redundancy check unit (CRC)

12.1 overview

In order to ensure safety during operation, the IEC61508 standard requires that data be confirmed even during CPU operation. This universal CRC performs CRC operations as a peripheral function. The universal CRC is not limited to the code flash memory area and can be used for multi-purpose inspection. Specify the data to be confirmed by the program.

12.2 characteristic

The CRC-generated polynomial uses CRC-16-CCITT's "$X^{16}+X^{12}+X^5+1$".

12.3 Feature description

After writing the CRCIN register, a PCLK clock is needed to save the CRC operation result to the CRCD register. If necessary, you need to read the data of the previous operation before writing, otherwise it will be overwritten by the new operation result.

Here's an example:

Sending data 0x12345678, starting from LSB to MSB complete.

The order in which it was sent	0001_1110	0110_1010	0010_1100	0100_1000	Sends on a bitwise basis from left to right
	↓	↓	↓	↓	Bitwise in reverse order in bytes
Reverse order results	0111_1000	0101_0110	0011_0100	0011_0010	
CRCIN data	0x78 ->	0x56 ->	0x34 ->	0x12	Enter the data into the CRCIN
	↓				The polynomial is performed 4 times
CRC results	0000_1000_1111_0110				
↓					
CRCD data	0x08F6				hexadecimal

Taking into account the LSB-preferred communication method, the bit order of the input data is first reversed and then calculated. Send data "0x12345678" from LSB, following "0x78", "0x56", "0x34", "0x12" The order of the WRITE registers is written, and finally the value is read from the CRCD register as "0x08F6". This is the result of a CRC operation after reversing the bit order of the "0x12345678" of the data.

12.4 Register mapping

(CRC base address = 0x4A00_0000).

RO: read-only, WO: write-only, R/W: read-write

register	Offset	R/W	description	Reset value
CRCIN	0x000	R/W	CRC input register	0x0
CRCD	0x004	R/W	CRC data registers	0x0

12.5 Register description

12.5.1 CRC Input Register (CRCIN)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	CRCIN	The CRC input requires 8 bits of data to be calculated	0x0

12.5.2 CRC Data Register (CRCD)

bit	symbol	description	Reset value
31:16	-	Reserved	-
15:0	CRCD	The CRC holds the 16-bit result of the operation	0x0

13. Divider (HWDIV)

13.1 overview

The chip contains a32-bit/32-bit hardware divider.

13.2 characteristic

- Supports division of unsigned/signed numbers.
- Both the quotient and the remainder are 32 bits wide.
- The divide-by-zero flag indicates the bit.
- The fastest operations completion within 6 HCLK clock.
- Writing divisor register initiates division.

13.3 Function description

The divider can select signed mode or unsigned mode through register HWDIVCON[1], and the divider quotient register HWDIVQ and the remainder register HWDIVR can save the complement of the operation result in signed mode HWDIVCON[1]; It is possible to determine whether the divisor is 0 by register HWDIVCON[2], which is a read-only bit; At the same time, the divider can be determined by register HWDIVCON[3], which is a read-only bit, and a read value of 0 indicates that the divider is operating, 1 indicates that the divider is complete, and the bit is also 1 when the divider is idle.

Note that the clock enable bit of the divider is set in register APBCKEN.

13.4 Register mapping

(HWDIV base address = 0x5500_0000).

RO: read-only, WO: write-only, R/W: read-write

register	Offset	R/W	description	Reset value
CON	0x000	R/W	Divider control registers	0x0
DIVD	0x004	R/W	Divider dividend registers	0x0
DIVS	0x008	R/W	Divider divisor register	0x0
DIVQ	0x00C	RO	Divider operation result quotient	0x0
DIVR	0x010	RO	Remainder of the result of the divider operation	0x0

13.5 Register description

13.5.1 Divider Control Register (HWDIVCON)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3	READY	The divider completes the indicator bit 0: Divider operation 1: The divider is complete or in idle	0x0
2	DIVBY0	Divider divide-zero indicator bit 0: The divisor is not 0 1: The divisor is 0 (The bit is automatically updated after the division operation is completed).	0x0
1	SIGN	The divider symbol selects the bit 0: Unsigned mode 1: Signed mode	0x0
0	-	Reserved	-

13.5.2 Divider dividend register (HWDIVD)

bit	symbol	description	Reset value
31:0	DIVIDEND	32 bits are divised	0x0

13.5.3 Divider divisor register (HWDIVS)

bit	symbol	description	Reset value
31:0	DIVISOR	32-bit divisor	0x0

13.5.4 Divider quotient register (HWDIVQ)

bit	symbol	description	Reset value
31:0	QUOTIENT	The result quotient of a 32-bit division operation	0x0

13.5.5 Divider remainder register (HWDIVR)

bit	symbol	description	Reset value
31:0	REMAINDER	The remainder of the result of a 32-bit division operation	0x0

14. Timer (TIMER0/1)

14.1 overview

Two programmable 32-bit/16-bit counters, namely TIMER0 and TIMER1, provide users with a convenient timing counting function.

14.2 characteristic

- Configurable 32-bit/16-bit down counter.
- Each timer has a separate prescaler.
- Provides three counting operation modes: single trigger, cycle counting, and continuous counting.
- Supports chip wake-up from sleep mode.

14.3 Feature description

14.3.1 Single trigger mode

If the timer is operating in single trigger mode, after enabling the timer, the counter loads the initial value from the loading register, counts down, and when the counter is decremented to 0, it stops working and produces an interrupt. To start the single trigger mode again, you need to zero out the TMROS bit and then set the TMROS bit.

(When starting the single trigger mode again, it should be noted that when the TMROS bit is cleared, the time to remain 0 must be greater than a timer count period)

14.3.2 Cycle count mode

If the timer works in cycle count mode, after enabling the timer, the counter loads the initial value from the loading register and counts down, and when the counter decreases to 0, the counter loads the initial value from the loading register and continues counting, while producing an interrupt.

14.3.3 Continuous count mode

If the timer works in continuous count mode, after enabling the timer, the counter loads the initial value from the loading register, counting down, and when the counter is decremented to 0, the counter loads the maximum value as the initial value and continues counting while generating an interrupt.

14.3.4 Lazy loading feature

When data is written to the load register, the counter does not continue to decrement, it loads the initial value from the load register on the rising edge of the next TIMER_CLK, and then decrements the count.

When data is written to the lazy load register, the data is written to the load register on the rising edge of the next TIMER_CLK, and if the counter has begun to count, it waits for the current cycle count to be 0 before loading the initial value from the load register.

14.4 Register mapping

(Timer0 base address = 0x4680_0000; Timer1 base address = 0x4680_0100).

RO: read-only; WO: Write only; R/W: read and write;

register	Offset	R/W	description	Reset value
WITH	0x000	R/W	Timer control register	0x20
LOAD	0x004	R/W	Timer loading register	0x0
VAL	0x008	RO	Timer current value register	0xFFFFFFFF
RICE	0x00c	RO	Timer interrupt source status register	0x0
PUT	0x010	RO	Timer enabled Interrupt status register	0x0
ICLR	0x014	WO	Timer interrupt clear register	-
BGLOAD	0x018	R/W	Timer delay loading register	0x0

14.5 Register description

14.5.1 Timer control register (TIMERxCON)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7	TMREN	Timer enable bit 0: Disable 1: Enable	0x0
6	TMRMS	Timer mode select bit 0: Continuous count mode 1: Cycle count mode	0x0
5	TMRIE	Timer interrupt enable bit 0: Disable Interrupt 1: Enable interrupt	1
4	-	Reserved	-
3:2	TMRPRE	Timer prescale 00: Divide-by-1 01: Divide-by-16 10: Divide by 256 11: Reserved	0x0
1	TMRSZ	Timer count bit selection 0: 16-bit counter 1: 32-bit counter	0x0
0	TMROS	Single trigger mode select bit 0: The mode is determined by the TRMS bit 1: Single-shot trigger mode (Single-shot mode is triggered again, the initial value of which is determined by the TRMS bit)	0x0

14.5.2 Timer loading register (TIMERxLOAD)

bit	symbol	description	Reset value
31:0	TMRxLOAD	Timer loading registers	0x0

14.5.3 Timer current value register (TIMERxVAL)

bit	symbol	description	Reset value
31:0	TMRxVAL	The timer current count value	0xFFFFFFFF

14.5.4 Timer interrupts the source status register (TIMERxRIS)

bit	symbol	description	Reset value
31:1	-	Reserved	-
0	TMRxRIS	The timer interrupts the source state 1: An interrupt is generated 0: No interrupt was generated	0x0

14.5.5 The timer enabled Interrupt status register (TIMERxMIS)

bit	symbol	description	Reset value
31:1	-	Reserved	-
0	TMRxMIS	The timer enabled Interrupt status bit 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0x0

14.5.6 Timer interrupt clear register (TIMERxICLR)

bit	symbol	description	Reset value
31:0	TMRxICLR	Write any number, clear the timer interrupt	-

14.5.7 Timer delay loading register (TIMERxBGLOAD)

bit	symbol	description	Reset value
31:0	TMRxBGLOAD	The timer lazy load register (the read value is the value of the last time TMRxLOAD or TIMERxBGLOAD was written).	0x0

15. Capture/Compare/Pulse Width Modulation Module (CCP0/1)

15.1 overview

It contains 2 groups of CCP modules CCP0/CCP1, and each group of CCP corresponds to A and B two channels. CCP0 corresponds to CCP0A/CCP0B, and CCP1 corresponds to CCP1A/CCP1B.

15.2 characteristic

- Up to 2 ccps with up to 4 PWM outputs.
- Each set of CCPs can be set with an independent period.
- CCPn has an internal 16-bit counter that generates a compare/overflow interrupt.
- The CCPn has a stand-alone capture function and can optionally input signals at the A or B pins.
- CCP1 has a 4-channel capture function that can simultaneously capture CCP0A/CCP0B/CCP1A/CCP1B input signals.
- Capture mode 1 supports the reload CCP0 counter function for capture operations.
- The internal channel CAP3 supports analog comparator output capture.
- Internal channel CAP0-CAP3 supports software capture functionality.

15.3 Feature description

15.3.1 Pulse width modulation mode (PWM)

Each set of CCP can output A and B two PWMs: PWMxA, PWMxB, these two channels share a cycle, the output duty cycle can be set independently through CCPDxA, CCPDxB. PWMxA/PWMxB output polarity can be set by PWMxAO/PWMxBOP bits, corresponding to CCPxA/ CCPxB channel output.

When CCPx run bit is set to 1, the 16-bit counter loads the value of the CCPx reload register, counts down, and when the count value is equal to the value of CCP DxA/B, the PWMxA/PWMxB output level changes.

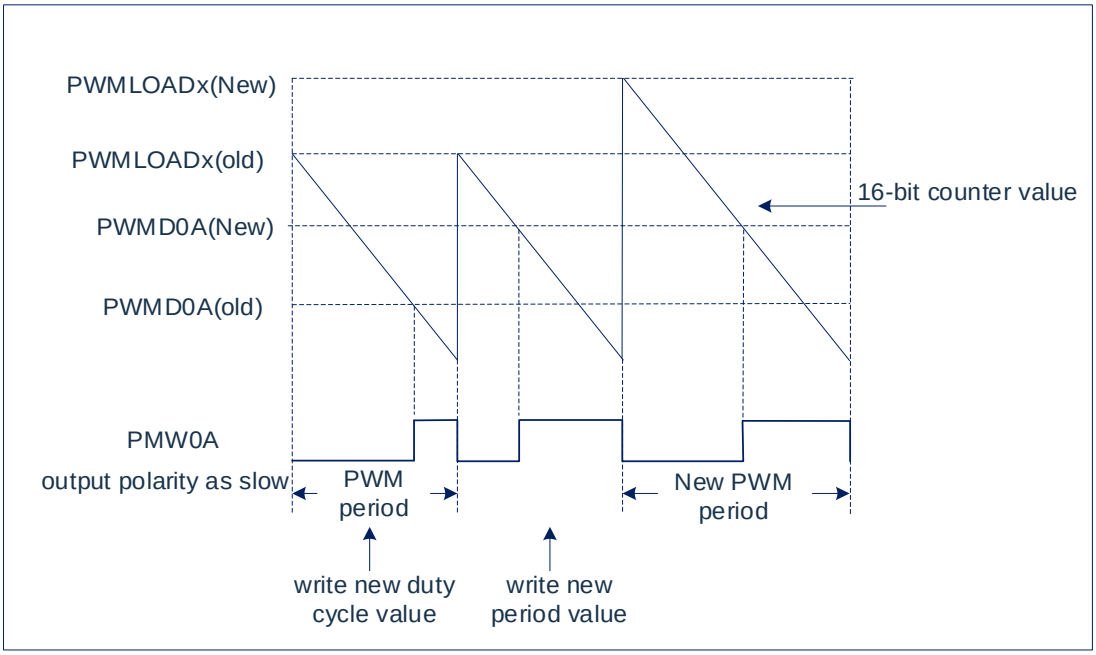


Figure 15-1: PWM timing diagram

Periods and duty cycles are calculated as follows:

Period = CCPLOAD× CCP clock period

PWMxA duty cycle = CCPDxA/CCPLOADx (supports 0%~100%)

PWMxB duty cycle = CCPDxB/CCPLOADx (supports 0%~100%)

When CCP LOADx=0, PWMxA, PWMxB duty cycle is 0%.

WHEN CCPDxA> CCPLOADx is, the duty cycle is 100%.

15.3.2 Capture mode 0

The capture mode is external capture.

Each set of CCP can be set from A or B as an external capture signal pin, after the CCPRUNx is set, the 16-bit count starts from the 0xFFFF and counts down, when the capture condition is triggered, the counter stops counting, and the CCPxA or CCPxB returns the value of the current counter. If you need to perform the next capture, you need to clear the CCP RUNx and then set it.

The capture time is calculated as follows:

CCPLOADx.RELOAD=0, capture time=(0xFFFF -CCPDxA/B) ×CCPx clock period

CCPLOADx.RELOAD=1, Capture Time=(CCPxLOAD[15:0]-CCPDxA/B) × CCPx clock period

15.3.3 Capture mode 1

CCP1 includes 4 internal channels such as CAP0, CAP1, CAP2, CAP3. One of the channels can be selected as the capture channel either in the external channel ECAP00-03 or ECAP10-13. You can also select CCP0A/CCP0B/CCP1A/CCP1B as the capture channels.

ECAP00-03 corresponds to the positive input C0P0-C0P3 of analog comparator0.

The ECAP10-13 corresponds to the positive input C1P0-C1P3 of analog comparator1.

When using ECAP external capture, the corresponding port needs to be set to GPIO function.

When using CCP0A/CCP0B/CCP1A/CCP1B capture, the corresponding port needs to be set as a CCP port.

Correspondence of CAPn to external channels:

Internal channels	External channels
CAP0	CAP0CHS=n: Select ECAP0n (n=0-3) @ECAPS=0 CAP0CHS=n: Select ECAP1n (n=0-3) @ECAPS=1 CAP0CHS=F: Select CAP0A CAP0CHS = Other values: Reserved
CAP1	CAP1CHS=n: Select ECAP0n (n=0-3) @ECAPS=0 CAP1CHS=n: Select ECAP1n (n=0-3) @ECAPS=1 CAP1CHS=F: Select CAP0B CAP1CHS = Other values: Reserved
CAP2	CAP2CHS=n: Select ECAP0n (n=0-3) @ECAPS=0 CAP2CHS=n: Select ECAP1n (n=0-3) @ECAPS=1 CAP2CHS=F: Select CAP1A CAP2CHS = Other values: Reserved
CAP3	CAP3CHS=n: Select ECAP0n (n=0-3) @ECAPS=0 CAP3CHS=n: Select ECAP1n (n=0-3) @ECAPS=1 CAP3CHS=8: Select the ACMP0 filter to select the output after selection CAP3CHS=9: Select ACMP1 Filter to select the output after selection CAP3CHS=F: Select CAP1B CAP3CHS = Other values: Reserved

In capture mode 1, PWM mode outputs for CCP0 and CCP1 and external capture mode 0 are disabled.

This mode requires CCP1 to operate in count mode, and the capture operation loads the CCP1 count median into the associated registers.

In addition, CCP0 can optionally operate in count mode, and the CAP0-CAP3 capture trigger loading function can be set separately. That is, when the channel is set up to have a capture operation generated, the counter initial value of CCP0 will be reloaded. Multiple channels can set the function at the same time, and software-triggered capture does not reload the initial value of CCP0.

In capture mode 1, the compare/overflow interrupt function of CCP0 andCCP1 can be used normally.

There are two types of capture methods: an external signal trigger capture and a software trigger capture.

1) External signal trigger capture:

Both CAP0-CAP3 can be selected for rising/falling edge or double edge capture. When a signal is generated, the value of the CCP1 counter is captured into the corresponding register and an interrupt flag is generated. The correspondence of the 4 channels to the capture register is as follows:

CAP0/CAP1/CAP2/CAP3 correspond to cap0DAT/CAP1DAT/CAP2DAT/CAP3DAT registers, respectively.

2) Software triggered capture:

Write operations to CAP0DAT-CAP3DAT generate capture operations on the CAP0-CAP3 channels. Capture the value of the CCP1 counter to the corresponding register. And the 31-16 bits written must be 0x55AA to trigger the capture operation. The low 16-bit data written is not correlated. Software-triggered capture does not produce an interrupt flag.

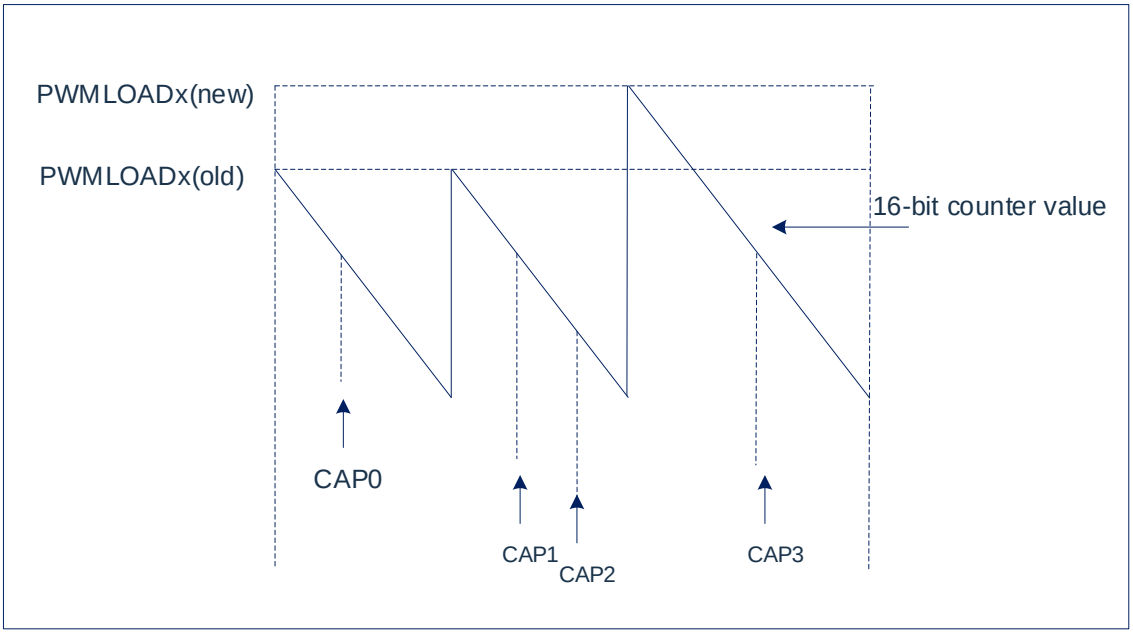


Figure 15-2: CAP0-CAP3 channel capture operation

15.3.4 PWM configuration process

- Configure the PWM control registers, set the prescale, select the PWM mode, and enable PWM.
- Configure the PWM cycle to write to the CCPLOADx registers.
- Configure the PWM duty cycle to write to the CCPDxA/CCPDxB registers.
- If an interrupt is required, enable the associated interrupt bits and clear the interrupt status register.
- Set the corresponding I/O port to the PWM output.
- Set the PWM run register to start the output.

15.3.5 interrupt

In PWM mode, CCPx can generate two types of interrupts:

- When the counter is decremented to 0, an underflow interrupt is generated.
- A comparison interrupt occurs when the value of the counter is equal to the value of CCPDxA or CCPDxB.

At capture mode 0/1, two types of interrupts can be generated:

- When the counter is decremented to 0, an underflow interrupt is generated.
- When a capture condition is triggered, a capture interrupt is generated.

15.4 Register mapping

(CCP base address = 0x4280_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
CCPCON0(P1B)	0x000	R/W	CCP0 control register	0x0
CCPLOAD0(P1A)	0x004	R/W	CCP0 reload register	0x0
CCPD0A(P1A)	0x008	R/W	CCP0 Channel A Data Register	0x0
CCPD0B(P1A)	0x00c	R/W	CCP0 channel B data register	0x0
CCPCON1(P1B)	0x010	R/W	CCP1 control register	0x0
CCPLOAD1(P1A)	0x014	R/W	CCP1 reload register	0x0
CCPD1A(P1A)	0x018	R/W	CCP1 Channel A data register	0x0
CCPD1B(P1A)	0x01C	R/W	CCP1 channel B data register	0x0
-	0x030	-	Reserved	-
-	0x034	-	Reserved	-
-	0x038	-	Reserved	-
-	0x03C	-	Reserved	-
CCPIMSC(P1B)	0x040	R/W	CCP interrupt enable register	0x0
CCPRIS	0x044	RO	CCP interrupt source status register	0x0
CCPMIS	0x048	RO	THE CCP enabled Interrupt status register	0x0
CCPICLR	0x04C	WO	CCP interrupt clear register	0x0
CCPRUN(P1B)	0x050	R/W	CCP run register	0x0
CCPLOCK	0x054	R/W	CPP0/1 write enable register	0x0
CAPCON(P1B)	0x058	R/W	Capture control register	0x0
CAPCHS(P1B)	0x05C	R/W	Capture channel selection register	0x0
CAP0DAT0(P1A)	0x060	R/W	Capture channel 0 data register	0x0
CAP1DAT0(P1A)	0x064	R/W	Capture channel 1 data register	0x0
CAP2DAT0(P1A)	0x068	R/W	Capture channel 2 data register	0x0
CAP3DAT0(P1A)	0x06C	R/W	Capture channel 3 data register	0x0

Note:

1) (P1A/P1B) The registers marked are protected registers.
2) (P1A): When LOCK=55H or AAH, the marked register allows writing; = Other values, forbidden to write.
3) (P1B): When LOCK=55H, the labeled register is allowed to write; = Other values, forbidden to write.

15.5 Register description

15.5.1 CCPx control register (CCPCONx) (x=0,1)

bit	symbol	description	Reset value
31:7	-	Reserved	-
6	CCPxEN	CCPx enable bit 0: Disable 1: Enable	0x0
5:4	CCPxPS	CCPx Prescale selection 0x0: PCLK 0x1: PCLK/4 0x2: PCLK/16 0x3: PCLK/64	0x0
3	CCPxMS	CCPx mode selection 0: Capture mode 0 (effective when CAPEN=0). 1: PWM mode (effective when CAPEN=0).	0x0
2	CCPxCM0CS	CCPx capture mode 0 capture channel selection 0: Channel CCPxA 1: Channel CCPxB	0x0
1:0	CCPxCM0ES	CCPx capture mode 0 capture mode selection 0x0: CCPRUNx=1 starts counting, rises along the capture and produces an interrupt 0x1: CCPRUNx=1 starts counting, drops along the capture and produces an interrupt 0x2: The rising edge starts counting, and the falling edge captures and produces an interrupt 0x3: The falling edge starts counting, and the rising edge captures and produces an interrupt	0x0

15.5.2 CCP reload register (CCPLOADx) (x=0,1)

bit	symbol	description	Reset value
31:17	-	Reserved	-
16	RELOAD	**CCP0 module:** PWM mode: Reload the enable bit 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP0LOAD Capture mode 0: 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP0LOAD **CCP1 module:** PWM mode: Reload the enable bit 0: The counter reload value is 0xFFFF 1: The counter reload value is CCP1LOAD Capture mode 0, 1: 0: The counter reload value is 0xFFFF	0x0

		1: The counter reload value is CCP1LOAD	
15:0	CCPxLOAD	The load value of the CCPx counter (the recommended load value is not 0).	0x0

15.5.3 CCPxA data register (CCPDxA) (x=0,1)

bit	symbol	description	Reset value
31:17	-	Reserved	-
16	PWMxAOP	PWMxA output polarity selection 0: Normal output 1: Inverting output	0x0
15:0	CCPxADATA	In PWM mode: The duty cycle of PWMx A When capture mode 0: Capture the results	0x0

15.5.4 CCPxB data register (CCPDxB) (x=0,1)

bit	symbol	description	Reset value
31:17	-	Reserved	-
16	PWMxBOP	PWMxB output polarity selection 0: Normal output 1: Inverting output	0x0
15:0	CCPxBDATA	In PWM mode: The duty cycle of PWMx B When capture mode 0: Capture the results	0x0

15.5.5 CCP Interrupt Enable Register (CCPIMSC)

bit	symbol	description	Reset value
31:12	-	Reserved	-
11	CAP3IMSC	CAP3 capture interrupt enable bits 0: Disable 1: Enable	0x0
10	CAP2IMSC	CAP2 capture interrupt enable bits 0: Disable 1: Enable	0x0
9	CAP1IMSC	CAP1 capture interrupt enable bits 0: Disable 1: Enable	0x0
8	CAP0IMSC	CAP0 capture interrupt enable bits 0: Disable 1: Enable	0x0
7:6	-	Reserved	-
5	PWMIMSC	PWM1 overflow interrupt enable bit 0: Disable 1: Enable	0x0
4	PWMIMSC4	PWM0 overflow interrupt enable bit 0: Disable 1: Enable	0x0
3:2	-	Reserved	-
1	PWMIMSC1	PWM1 compares/capture interrupt enable bits 0: Disable	0x0

		1: Enable	
0	PWMIMSC0	PWM0 compares/capture interrupt enable bits 0: Disable 1: Enable	0x0

15.5.6 CCP Interrupt Source Status Register (CCPRIS)

bit	symbol	description	Reset value
31:12	-	Reserved	-
11	CAP3RIS	CAP3 capture interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0x0
10	CAP2RIS	CAP2 capture interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0x0
9	CAP1RIS	CAP1 capture interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0x0
8	CAP0RIS	CAP0 capture interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0x0
7:6	-	Reserved	-
5	PWMRIS5	PWM1 overflow interrupt status bit 1: An interrupt is generated 0: No interrupt was generated	0x0
4	PWMRIS4	PWM0 overflows interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0x0
3:2	-	Reserved	-
1	PWMRIS1	PWM1 compares/capture interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0x0
0	PWMRIS0	PWM0 compares/capture interrupt status bits 1: An interrupt is generated 0: No interrupt was generated	0x0

15.5.7 CCP enabled Interrupt Status Register (CCPMIS)

bit	symbol	description	Reset value
31:12	-	Reserved	-
11	CAP3MIS	CAP3 has enabled the capture of interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0x0
10	CAP2MIS	CAP2 has enabled the capture of interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0x0
9	CAP1MIS	CAP1 has enabled capture of interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0x0
8	CAP0MIS	CAP0 has enabled capture of interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0x0
7:6	-	Reserved	-
5	PWMMIS5	PWM1 has enabled the overflow interrupt status bit 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0x0
4	PWMMIS4	PWM0 has enabled the overflow interrupt status bit 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0x0
3:2	-	Reserved	-
1	PWMMIS1	PWM1 has enabled the Compare/Capture interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0x0
0	PWMMIS0	PWM0 has enabled the Compare/Capture interrupt status bits 1: Interrupt enables and produces interrupts 0: No interrupt was generated	0x0

15.5.8 CCP Interrupt clear register (CCPICLR)

bit	symbol	description	Reset value
31:12	-	Reserved	-
11	CAP3ICLR	Write 1 to clear the CAP3 capture interrupt status bit	0x0
10	CAP2ICLR	Write 1 to clear CAP2 capture interrupt status bits	0x0
9	CAP1ICLR	Write 1 to clear CAP1 to capture interrupt status bits	0x0
8	CAP0ICLR	Write 1 to clear the CAP0 capture interrupt status bit	0x0
7:6	-	Reserved	-
5	PWMICLR5	Write 1 to clear the PWM1 overflow interrupt status bit	0x0
4	PWMICLR4	Write 1 to clear the PWM0 overflow interrupt status bit	0x0
3:2	-	Reserved	-
1	PWMICLR1	Write 1 clears the PWM1 compare/capture interrupt status bits	0x0
0	PWMICLR0	Write 1 to clear the PWM0 compare/capture interrupt status bits	0x0

15.5.9 CCP Run Register (CCPRUN)

bit	symbol	description	Reset value
31:2	-	Reserved	-
1	CCPRUN1	CCP1 operational control bit 0: Stop it 1: run	0x0
0	CCPRUN0	CCP0 operational control bit 0: Stop it 1: run	0x0

15.5.10 CCP write enable control register (CCPLOCK)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	LOCK	When LOCK=0xaa, enables the operation of registers with protection level P1A When LOCK=0x55, enables the operation of registers with protection levels P1B and P1A When LOCK=other values, operation of registers with a protection level is prohibited	0x0

15.5.11 CAP Control Register (CAPCON)

bit	symbol	description	Reset value
31:13	-	Reserved	-
12	CMONKEYS	Capture mode 1 enable bit 0: CCP0/CCP1 is enabled for PWM mode or capture mode 0 1: Capture mode 1 enables, which is full-channel capture mode CCP0 switches to a continuous count mode that can be set CCP1 toggles to a continuous count mode that can be set	0x0
11	CAP3RLEN	Capture mode 1 CAP3 captures the counter load enable bit that triggers CCP0 0: Disabled 1: Enabled, (requires capture mode 1 and is in effect inCCP0 operating state). CAP3 has a capture trigger signal, andCCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	0x0
10	CAP2RLEN	Capture mode 1 CAP2 captures the counter load enable bit that triggers CCP0 0: Disabled 1: Enabled, (requires capture mode 1 and is in effect inCCP0 operating state). CAP2 has a capture trigger signal, and CCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	0x0
9	CAP1RLEN	Capture mode 1 CAP1 captures the counter load enable bit that triggers CCP0 0: Disabled 1: Enabled, (requires capture mode 1 and is in effect inCCP0 operating state). CAP1 appears to capture the trigger signal, then CCP0 runs on the counter during the row, the data in the CCP0LOAD register is reloaded.	0x0
8	CAP0RLEN	Capture mode 1 CAP0 captures the counter load enable bit that triggers CCP0 0: Disabled 1: Enabled, (requires capture mode 1 and is in effect inCCP0 operating state). CAP0 has a capture trigger signal, andCCP0 will reload the data in the CCP0LOAD register during the operation of the counter.	0x0
7:6	CAP3ES	CAP3 capture mode selection 0x0: Disabled 0x1: Rising edge capture 0x2: Drop edge capture 0x3: Double edge	0x0
5:4	CAP2ES	CAP2 capture mode selection 0x0: Disabled 0x1: Rising edge capture 0x2: Drop edge capture 0x3: Double edge	0x0
3:2	CAP1ES	CAP1 capture mode selection 0x0: Disabled 0x1: Rising edge capture 0x2: Drop edge capture	0x0

		0x3: Double edge	
1:0	CAP0ES	CAP0 capture mode selection 0x0: Disabled 0x1: Rising edge capture 0x2: Drop edge capture 0x3: Double edge	0x0

15.5.12 CAP Channel Selection Register (CAPCHS)

bit	symbol	description	Reset value
31:17	-	Reserved	-
16	ECAPS	ECAP capture channel group selection 0: Choose ECAP00-ECAP03 1: Choose ECAP10-ECAP13	0x0
15:12	CAP3CHS	CAP3 capture channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS). 0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: forbidden 0x5: forbidden 0x8: The output of ACMP0 (non-event output). 0x9: The output of ACMP1 (non-event output). 0xF: CCP1B Other values: Reserved	0x0
11:8	CAP2CHS	CAP2 capture channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS). 0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: forbidden 0x5: forbidden 0xF: CCP1A Other values: Reserved	0x0
7:4	CAP1CHS	CAP1 capture channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS). 0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: forbidden 0x5: forbidden 0xF: CCP0B Other values: Reserved	0x0
3:0	CAP0CHS	CAP0 captures channel selection 0x0: ECAPx0 (x = 0 or 1, determined by ECAPS Fixed).	0x0

		0x1: ECAPx1 0x2: ECAPx2 0x3: ECAPx3 0x4: forbidden 0x5: forbidden 0xF: CCP0A Other values: Reserved	

15.5.13 CAP data register (CAPnDAT0) (n=0-3)

bit	symbol	description	Reset value
31:16	-	Read: invalid Write: 0x55AA, a capture operation that produces CAPns Write: Other values are not valid	0x0
15:0	CAPnDATA	Read: Capture the 16 bit value of the CCP1 counter for CAPn Write: invalid	0x0

16. Enhanced PWM (EPWM)

16.1 overview

The enhanced PWM module supports six PWM generators, which can be configured as six independent PWM outputs (EPWM0-EPWM5) or as three pairs of complementary PWM (EPWM0-EPWM1, EPWM2-EPWM3, EPWM4-EPWM5) with programmable dead-zone generators.

Each pair of PWMs shares an 8-bit prescaler with 6 clock dividers that provide 5 divider factors (1, 1/2, 1/4, 1/8, 1/16). Each PWM output is controlled by a separate 16-bit counter, and a 16-bit comparator is used to adjust the duty cycle. The 6-channel PWM generator provides 28 interrupt flags, and the period or duty cycle of the relevant PWM channel matches the counter and will produce interrupt flags, with each PWM having a separate enable bit.

Each PWM can be configured as a single mode (which generates a PWM signal cycle) or a cyclic mode (continuous output of the PWM waveform).

16.2 characteristic

The Enhanced PWM Module has the following features:

- 6 independent 16-bit PWM control modes.
  - 6 independent outputs: EPWM0, EPWM1, EPWM2, EPWM3, EPWM4, EPWM5;
  - 3 sets of complementary PWM pairs: (EPWM0-EPWM1), (EPWM2-EPWM3), (EPWM4-EPWM5), programmable dead-zone can be inserted;
  - 3 sets of synchronous PWM pairs: (EPWM0-EPWM1), (EPWM2-EPWM3), (EPWM4-EPWM5), each set of PWM pairs pin synchronization.
- Support group control, EPWM0, EPWM2, EPWM4 output synchronization, EPWM1, EPWM3, EPWM5 output synchronization.
- Single mode (edge alignment only) or auto-load mode.
- Support edge alignment, center alignment 2 modes.
- Center alignment mode supports symmetric and asymmetric counts.
- Programmable dead-zone generators are supported in complementary PWMs.
- Each PWM has independent polarity control.
- Hardware brake protection (external BKIN trigger, support software trigger).
- The ADC comparison event triggers hardware brake protection.
- The ACMP analog comparator triggers hardware brake protection
- The PWM edge or period can trigger the initiation of the AD conversion.

16.3 Feature description

Description of the relevant name:

- Period point: When the counter CNTn is counted to equal to the period PERIODn, it is called the period point. The resulting interrupt is PIFn.
- Zero point: When the counter CNTn counts to 0, it is called the zero point. The resulting interrupt is ZIFn.
- Up-compare point: When the counter CNTn is counted to equal to CMPDATn, it is called the up-compare point. The resulting interrupt is UIFn. Edge alignment counts have no up-compare points.
- Down-compare point: When the counter CNTn is subtracted to equal to CMPDATn or CMPDDATn, it is called a down-compare point. The resulting interrupt is DIFn.
- Midpoint: The midpoint is the middle point, and when the midpoint is centered on the counting method, the CNTn counts to a moment equal to the CMPDATn or CMPDDATn, and because the CNTn will be subtracted to 0, the moment is called the midpoint, which is also the period point. Edge alignment count has no midpoint, but has a period point.

Note:

1) When the edges are aligned, the period data is loaded at the beginning of the first count, which will produce a period point; At other moments, after the counter counts to 0, the period data needs to be loaded immediately. So the subsequent period point is the same as the position of the zero point. There is a down comparison point for this alignment, not an up comparison point.
2) When the center is aligned, the first count starts counting upwards from 0 and results in a zero point. When the period data is counted, a period point (midpoint) is generated. The zero point alternates with the midpoint. The alignment has an upward comparison point and a downward comparison point, and when the symmetry is counted, the upward comparison point and the downward comparison point are determined by CMPDATn; For asymmetric counting, the upward comparison point is determined by CMPDATn and the downward comparison point is determined by CMDDATn.

16.3.1 Block diagram

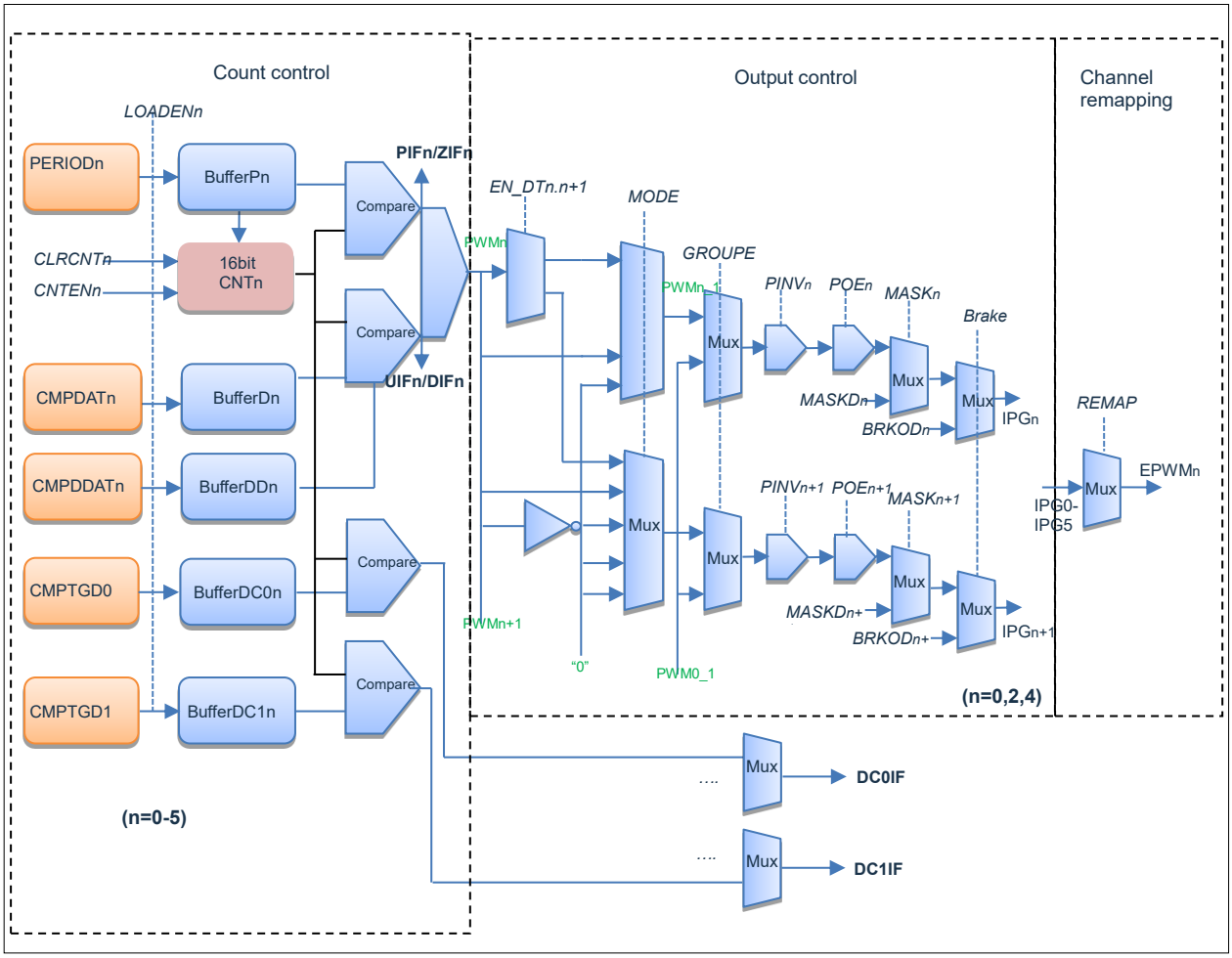


Figure 16-1: The signal of IPGn is the signal before the EPWMn remapping.

16.3.2 Clock divider

Each pair of PWMs shares an 8-bit prescaler, and after the prescale, each PWM can choose (1, 1/2, 1/4, 1/8, 1/16) 5 divider ratios.

PWM_CLK = PCLK / (CLKPSCxx + 1) / CLKDIVn, where xx can be 01, 23, 45, n=0-5.

16.3.3 Independent output mode

The six EPWM channel outputs do not affect each other and operate according to their respective cycle/duty cycle data.

16.3.4 Complementary output modes

In the complementary output mode, the six PWMs are divided into 3 pairs, EPWM0 is 1 pair with EPWM1, EPWM2 is 1 pair with EPWM3, and EPWM4 is 1 pair with EPWM5. There are 3 pairs of PWM in total.

EPWM0-EPWM1 operates on epwm0's period/duty cycle data, and EPWM0 is inverted from the EPWM1 waveform.

EPWM2-EPWM3 operates on epwm2's period/duty cycle data, and EPWM2 is inverted from the EPWM3 waveform.

EPWM4-EPWM5 operates on epwm4's period/duty cycle data, and EPWM4 is inverted from the EPWM5 waveform.

In this mode, the EPWM1/EPWM3/EPWM5 outputs are independent of their own associated operating data registers, but the output control is still valid. Such as output enable, mask, brake and other controls.

Dead-zone delay control is supported in complementary mode.

16.3.5 Synchronous output mode

In synchronous output mode, the six PWMs are divided into 3 pairs, EPWM0 is paired with EPWM1, EPWM2 is paired with EPWM3, and EPWM4 is paired with EPWM5. There are 3 pairs of PWM in total.

EPWM0-EPWM1 operates on the period/duty cycle data of EPWM0, which is in phase with EPWM1 waveform.

EPWM2-EPWM3 operates on the period/duty cycle data of EPWM2, which is in phase with EPWM3 waveform.

EPWM4-EPWM5 operates on the period/duty cycle data of EPWM4, which is in phase with EPWM5 waveform.

In this mode, the EPWM1/EPWM3/EPWM5 outputs are independent of their own associated operating data registers, but the output control is still valid. Such as output enable, mask, brake and other controls.

16.3.6 Grouped output mode

GROUPEN=1 enables the group function, 6 channels of PWM are divided into 2 groups, EPWM0, EPWM2, EPWM4 is 1 group, EPWM1, EPWM3, EPWM5 is another group.

EPWM0-EPWM2-EPWM4 operates on EPWM0's period/duty cycle data, with 3 channels in phase.

EPWM1-EPWM3-EPWM5 operates on EPWM0's period/duty cycle data, with 3 channels in phase.

When the grouping function is turned on, the EPWM2/EPWM4/EPWM3/EPWM5 outputs are independent of their own associated operating data registers, but the output control is still valid. Such as output enable, mask, brake and other controls.

16.3.7 Load update mode

There are two counter loading modes: Single mode and continuous mode (auto loading mode)

Single mode:

The period, duty cycle relevant data is loaded once at the beginning of the counter, and the output PWM period is related to the loading mode.

LoadTYPn=0, edge alignment is 1 period and center alignment is 0.5 periods.

When LOADTYPn=1, edge alignment is 2 periods and center alignment is 1 period.

LoadTYPn=2, edge alignment is 3 periods and center alignment is 1.5 periods.

At LOADTYPn=3, the edge alignment is 4 periods and the center alignment is 2 periods.

Continuous mode:

The period, duty cycle data is automatically loaded at the zero and midpoints of the PWM period. Midpoint loading exists only in center alignment count mode.

In edge alignment counting mode, a zero point is generated at the same time as a period point, and the count comparison circuit reloads the value of CMPDATn/PERIODn/CMPTGD0/CMPTGD1.

In center-align count mode, both the midpoint and the zero point are automatically loaded with values for the associated registers. Such a structure supports the first half waveform cycle duty cycle and the second half waveform cycle duty cycle.

Due to the dual cache structure of EPWM, during EPWM operation, the value of the relevant operating registers: CMPDATn/CMPDDATn/PERIODn/CMPTGD0/CMPTGD1 is changed, the PWM output waveform does not change immediately, and the values of these registers are loaded into the corresponding cache only at the zero or period point.

Such a structure does not immediately change the output waveform in the current PWM cycle or half-cycle after changing the period duty cycle data, and the PWM waveform will not change accordingly in the next cycle or half-cycle. That is, any changes in PWM-related data do not affect the current full PWM cycle or half-cycle.

In high-speed applications, it is possible that the load point has arrived, but the operation of writing to the operating register has not yet been completed. At this point, you do not expect some of the running data to have been loaded and another part of the running data to be unloaded.

For this high-speed application. The EPWM module provides a loading enable bit, after changing the relevant operating register, you need to set the load enable bit LOADENn to 1, and the LOADENn bit is automatically cleared after loading. This bit can also be read to determine whether the value of the associated register is loaded into the actual circuit. If LOADENn= 0, it means that it has been loaded, which will affect the PWM waveform being output; If LOADENn=1, it means that the current PWM waveform has not yet changed, and the value of the register that changed before the next load point will be loaded. If you change the value of the associated run register again, you also need to reset loadENn to 1.

By default, PWM loads the operating data of the relevant registers at both the zero and period points, and generates zero and periodic interrupts. In order to adapt to more flexible application requirements. PWM supports different loading modes and zero/period point interrupt generation.

In register EPWMCON3 LOADTYPn(0-5) can be set the load mode and the interrupt mode at the zero/period point:

LOADTYEn	Center alignment loading	Edge alignment loading
00	Each zero and period point is loaded with and produces zero and periodic interrupt flags	Each zero or period point is loaded with zero and periodic interrupt flags
01	Each zero point is loaded with a zero interrupt flag	Every 2 zeros are loaded with a zero interrupt flag
10	The first zero point is loaded alternately with the next cycle point, resulting in a zero and period point interrupt flag	Every 3 zeros or period points are loaded with a zero and periodic interrupt flag
11	Every two zeros are loaded with a relevant zero interrupt flag	Every 4 zeros are loaded with a zero interrupt flag

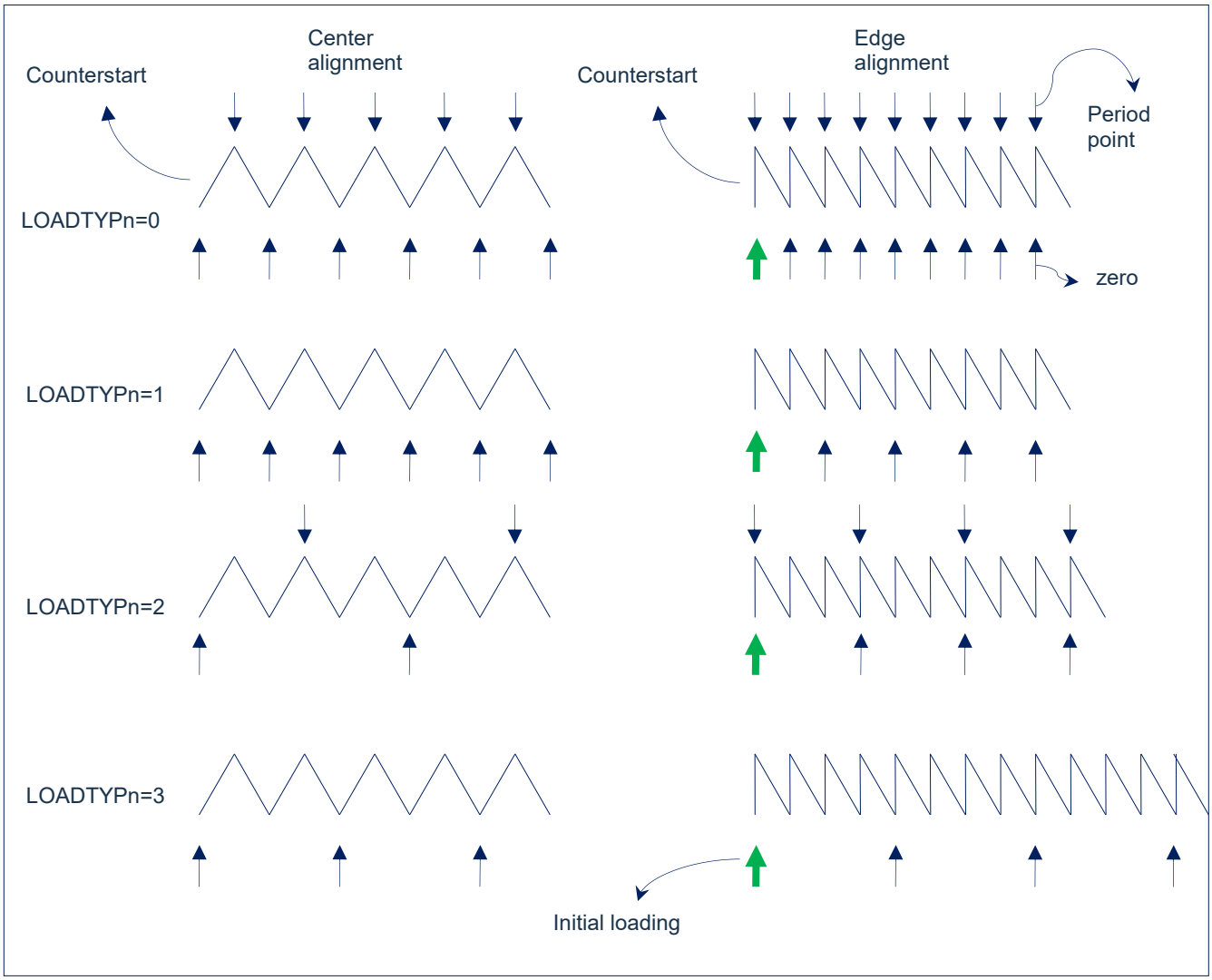


Figure 16-2:PWM period/duty cycle loading update block diagram

16.3.8 Edge alignment count mode

In edge alignment mode, the counting method is down, that is, minus 1 count. The 16-bit PWM counter CNTn counts down at the beginning of each cycle, compared to the latched CMPDATn value, and when CNTn= CMPDATn, the EPWMn output is high, cmPnDIF is set to 1. CNTn continues to count down to 0, at which point EPWMn will output low, the current CMPDATn and PERIODn will be reloaded at PWMnCNTM=1, and the PIF cycle interrupt flag will be set.

The relevant parameters for edge alignment are as follows:

High voltage duration=（CMPDATn+1）×Tpwm

$$\text{Period} = （\text{PERIODn+1}）\times \text{Tpwm}$$

$$\text{duty cycle} = \frac{\text{CMPDATn+1}}{\text{PERIODn+1}}$$

If CMPDATn > PERIODn, the duty cycle is 100%, and the EPWMn channel is always high. And there is no down-to-compare interrupt.

If CMPDATn= 0, the duty cycle is 0%.

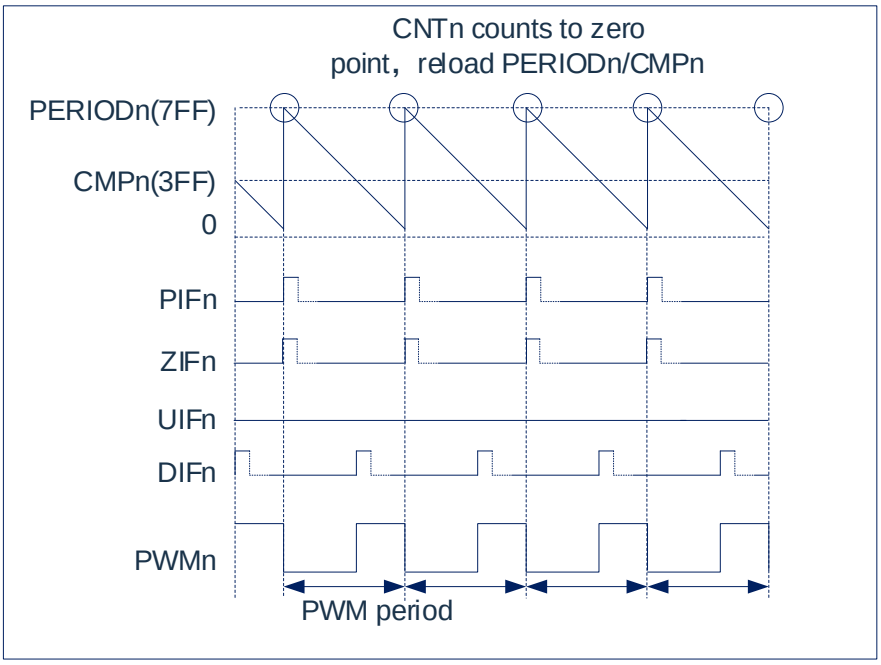


Figure 16-3: Edge alignment mode waveform plot

16.3.9 Center alignment count mode

In center-align mode, the counting method is counting up and then counting down.

The center alignment mode is divided into two symmetrical ways: symmetrical counting mode and asymmetric counting mode.

The symmetric count mode (ASYMEN=0) duty cycle is determined by CMPDATAn.

The asymmetric count mode (ASYMEN=1) duty cycle is determined by CMPDATAn and CMPDDATn.

Under the center-aligned symmetrical counting mode, the 16-bit PWM counter CNTn starts from 0 to count upwards, when CNTn = CMPDATn, EPWMn outputs a high level, after which CNTn continues to count upwards to equal to PERIODn, and then CNTn begins to count down, in the process of counting down CNTn= CMPDATn, EPWMn outputs a low level, and then continues to count down to 0.

$$High\ voltage\ duration = (PERIODn \times 2 - CMPDATn \times 2 - 1) \times Tpwm$$

$$Period = (PERIODn) \times 2 \times Tpwm$$

$$Duty\ Cycle = \frac{PERIODn \times 2 - CMPDATn \times 2 - 1}{PERIODn \times 2}$$

If CMPDATn > = PERIODn, the duty cycle is 0%, the EPWMn channel is always low, and there is no upward comparison interrupt or downward comparison interrupt.

If PERIODn=0, the duty cycle is 0%, the EPWMn channel is always low, and the zero-point interrupt and the period point interrupt are always present when CNTn is enabled.

If CMPDATn=0, the duty cycle is 100%.

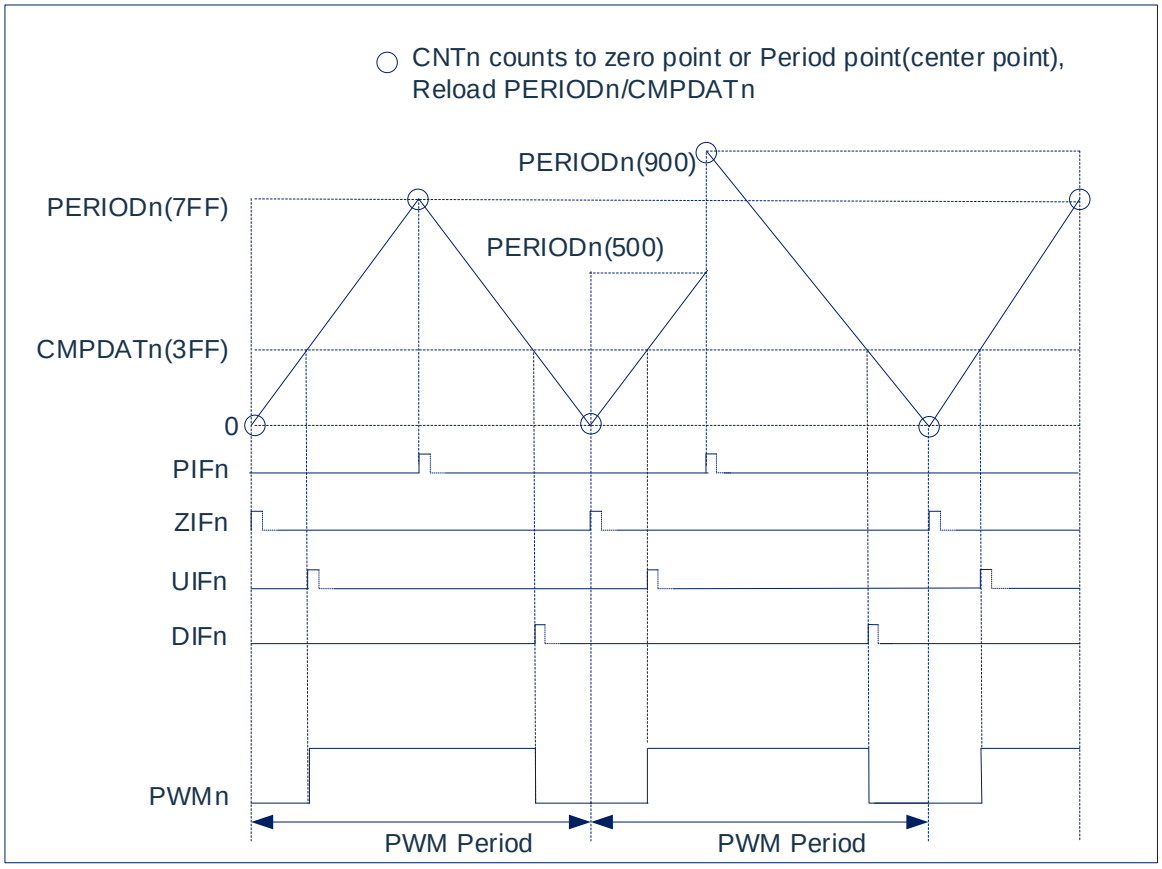


Figure 16-4: Center alignment mode symmetrical counting waveform plot

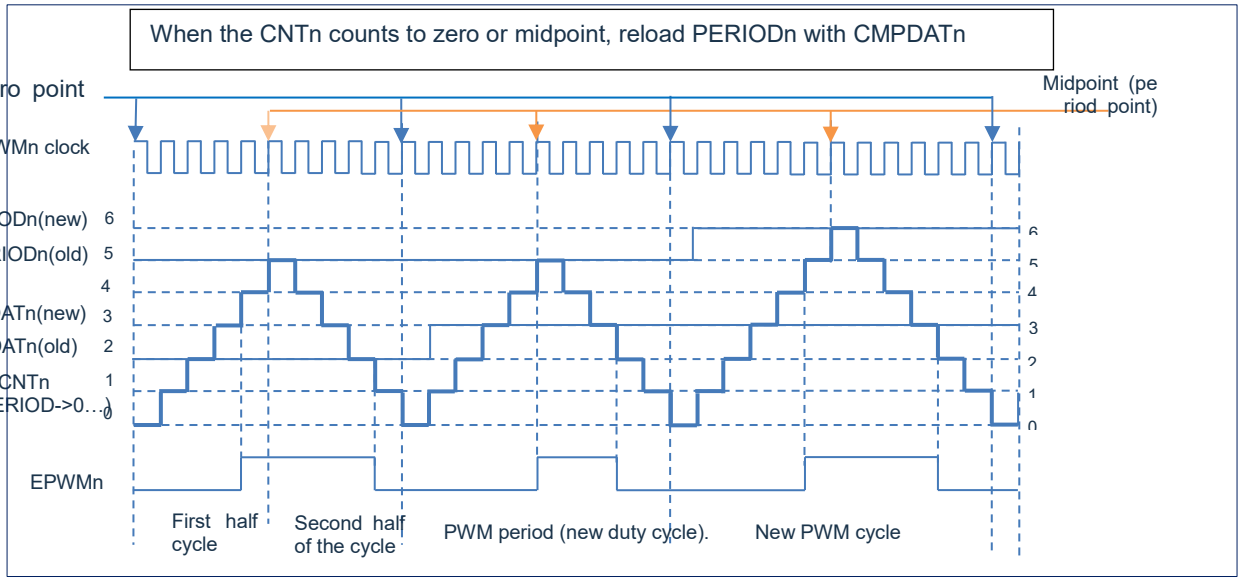


Figure 1 6-5: Center-aligned counter waveform (symmetrical count).

In the center-aligned asymmetric counting mode, the 16-bit PWM counter CNTn starts counting up from 0, when CNTn= CMPDATn, EPWMn outputs a high level, after which CNTn continues to count up to equal to PERIODn, and then CNTn begins to count down, in the process of counting down CNTn= CMPDDATn, EPWMn outputs a low level, and then continues to count down to 0. To enable the asymmetric counting method, the ASYMEN needs to be placed at 1, and the asymmetric counting method can achieve accurate center alignment waveforms.

The relevant parameters for the center-aligned asymmetric count are as follows:

High voltage duration = （PERIODn×2-CMPDDATn-CMPDATn-1）×Tpwm

Period = （PERIODn）×2×Tpwm

$$Duty\ Cycle = \frac{PERIODn\times 2-CMPDDATn-CMPDATn-1}{PERIODn\times 2},\quad (CMPDATAn<PERIODn, CMPDDATn<PERIODn)$$

$$Duty\ Cycle = \frac{PERIODn-CMPDDATn-1}{PERIODn\times 2},\quad (CMPDATAn\geq PERIODn, CMPDDATn<PERIODn)$$

$$Duty\ Cycle = \frac{PERIODn-CMPDATn}{PERIODn\times 2},\quad (CMPDATAn<PERIODn, CMPDDATn\geq PERIODn)$$

Duty Cycle =0%,（CMPDATAn≥PERIODn,CMPDDATn≥PERIODn）

CMPDATAn > =PERIODn does not produce an upward comparison interrupt.

CMPDDATAn does not produce a downward comparison interrupt when > =PERIODn.

If PERIODn=0, the duty cycle is 0%, the EPWMn channel is always low, and the zero-point interrupt and the period point interrupt are always present when CNTn is enabled.

If CMPDATn=0 and CMDATDn=0, the duty cycle is 100%.

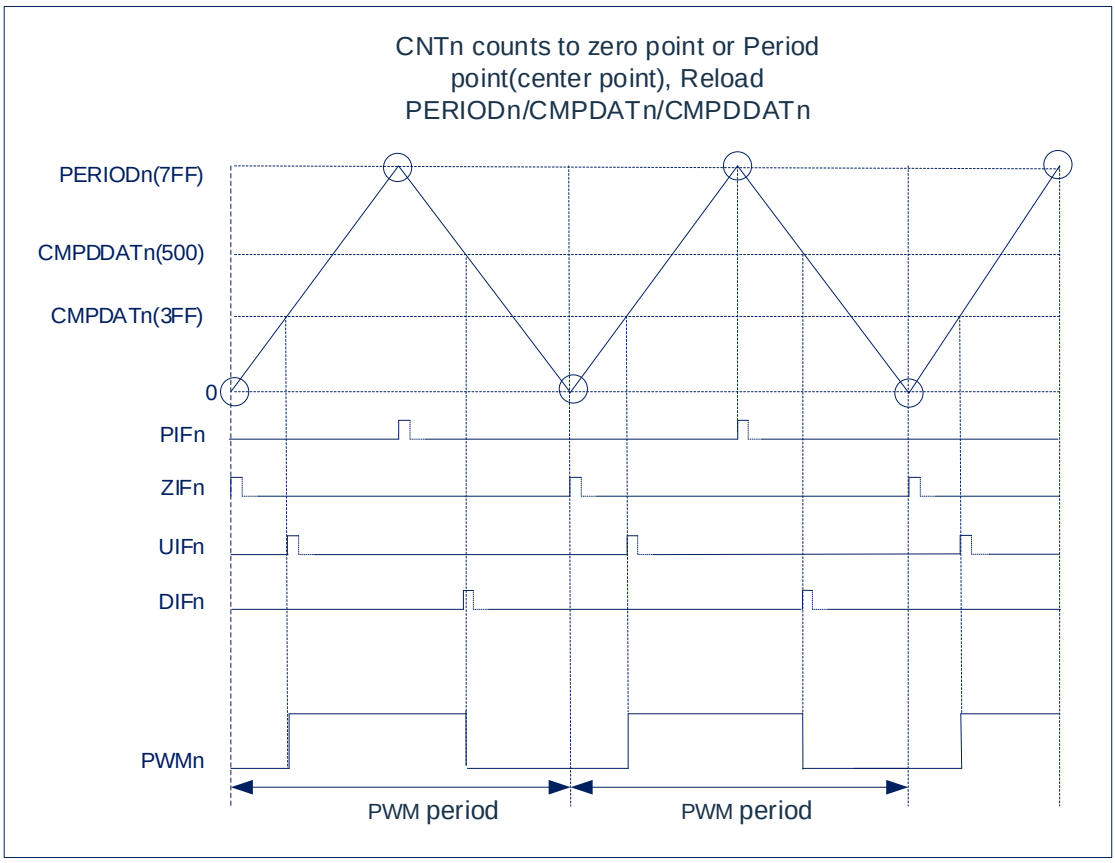


Figure 1 6-6: Asymmetric count waveform plot in center alignment mode

16.3.10 Independent counter comparison function

During the PWMn Channel Counter (CNTn) counter, two digital comparators are provided, and the counter CNTn is compared to the preset value, and if the counter value is equal to the preset value, an interrupt signal or an ADC operation can be triggered. This feature does not affect the output of the PWM.

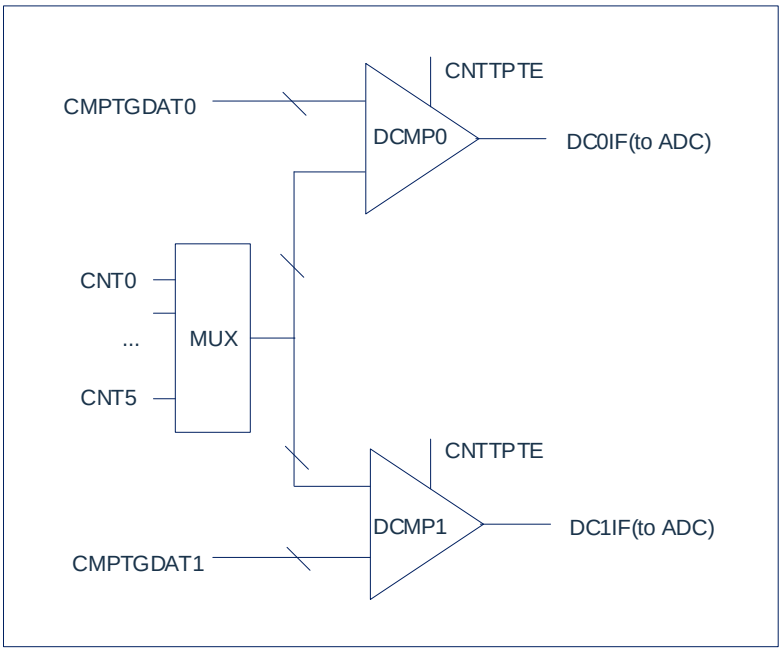


Figure 16-7: Independent counter comparison function

The digital comparator 0 compares the value of the counter CNTn with the value of CMPTGDAT0. If equal, an interrupt flag bit DC0IF is generated, cmPTGD0 [10:8] select one of the PWM0-5 channel counters to compare with CMPTGDAT0.

Digital comparator 1 compares the value of counter CNTn with the value of CMPTGDAT1. If equal, an interrupt flag bit DC1IF., CMPTGD1 [10:8] Select one of the PWM0-5 channel counters to compare with CMPTGDAT1

1) Edge alignment mode, how the digital comparator works:

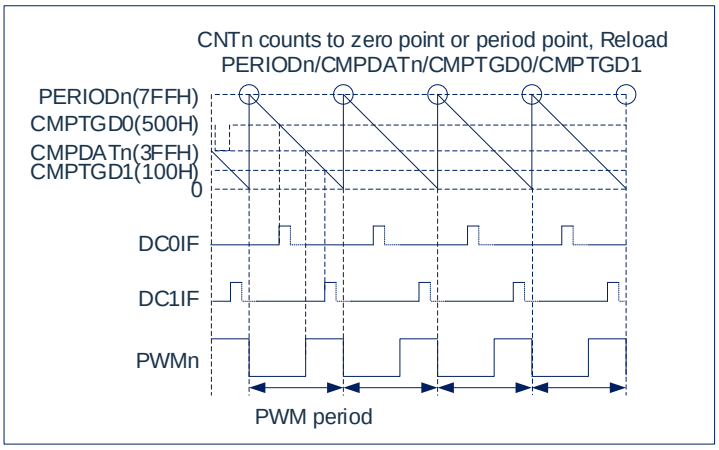


Figure 16-8: Edge alignment mode, how the digital comparator works

In edge counting mode, the digital comparator 0/1 can be set to produce a comparison interrupt at any counting moment.

2) Center alignment mode, how the digital comparator works:

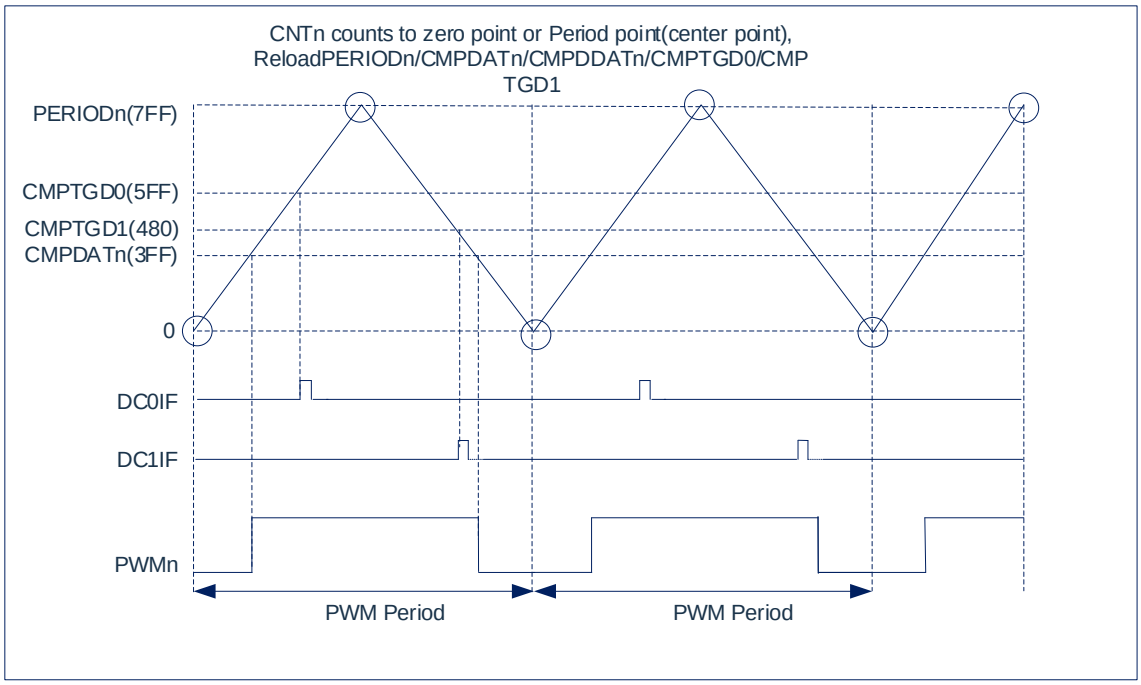


Figure 16-9: Center alignment mode, how the digital comparator works

In center-aligned count mode, the number comparator 0/1 can be set to be triggered by comparison in either up or down count mode. That is, both can be triggered in the first half of the cycle or the second half of the cycle, or one can be triggered in the first half of the cycle and the other in the second half of the cycle. Determined by CMPTGD0[19] bit CMPTGDSn.

16.3.11 Programmable dead-zone generator

The 6-channel PWM can be set to 3 sets of complementary pairs. In the complementary output mode, the period and duty cycle of PWM1, PWM3, and PWM5 are determined by the PWM0, PWM2, and PWM4 relevant registers, respectively, and the dead-zone delay registers can also affect the duty cycle of the PWM complementary pair. In addition to the corresponding output enable control bit (PWMnOE), the PWM1/PWM3/PWM5 output waveform is no longer controlled by its own registers.

In complementary mode, each set of complementary PWM pairs supports inserting a dead-zone delay, and the inserted dead-zone time is as follows:

PWM0/1 Dead-zone: (PWM01DT [9:0] +1) ×T_{PWM0}

PWM2/3 Dead-zone: (PWM23DT [9:0]+1) ×T_{PWM2}

PWM4/5 Dead-zone: (PWM45DT [9:0]+1) ×T_{PWM4}

T_{PWM0}/T_{PWM2}/T_{PWM4} are the clock source periods of PWM0/PWM2/PWM4, respectively.

Dead-zone time can be set from 0.021us to 21us (Fpwmn=48MHz)

The output mode does not affect the counter's mode, so both center alignment and edge alignment support complementary output modes.

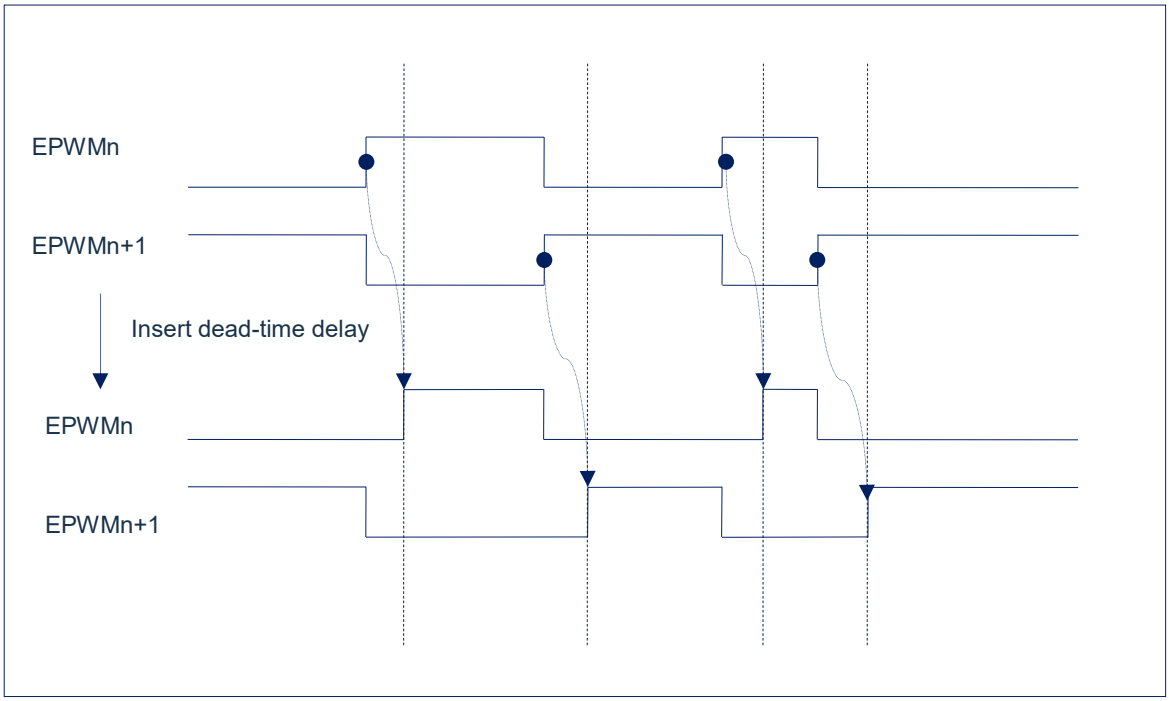


Figure 16-10: Both center alignment and edge alignment support complementary output modes

16.3.12 Mask and mask preset functions

EPWM supports masking functionality. EPWM0-EPWM5 has a separate control for each channel, and the corresponding control bits of EPWMn are MASKENn, MASKDn (in register MASK).

When MASKENn=0, the EPWMn channel outputs a normal PWM waveform;

When MASKENn=1, the EPWMn channel outputs the data of MASKDn;

The mask function's control register, THE MASK, also supports the ability to automatically load preset values. Turning on this function requires the output control register POEN at MASKLE bit set to 1, allowing MASK to automatically load the value of the MASKNXT register while disabling writing the MASK register.

Load time in POEN MASKLS < 2:0 > setting, with the option to have the same period/duty cycle (load point) as one of the EPWM0-EPWM5.

16.3.13 Hall sensor interface function

EPWM considers an interface with Hall sensors. An internal HALL position status detection circuit is included that detects the filtered level of the internal capture channels CAP0, CAP1, and CAP2 in the CCP0/1 module.

The presence state of the detection circuit after internal processing is called HALLST:

Hallst has 8 states, which correspond to the HALL position state as follows:

HALLST	The corresponding status
000	Hall detects that the circuit is not started or in its initial state
001	{CAP2-CAP0}=001
010	{CAP2-CAP0}=010
011	{CAP2-CAP0}=011
100	{CAP2-CAP0}=100
101	{CAP2-CAP0}=101
110	{CAP2-CAP0}=110
111	{CAP2-CAP0} the wrong state or sequence of errors during a change

The value of HALLST can be read out from the MASKNXT register, and the HALL position or sequence state can be determined at any time.

The HALL status detection sequence supports the following two types ({CAP2, CAP1, CAP0} order of occurrence):

1) ……-6-2-3-1-5-4-6-……
2) ……-6-4-5-1-3-2-6-……

If other sequences are considered to have been errors, HALLST will stop detecting after entering the state of 111. At the same time, the interrupt flag HALLIF will be generated. If you need to restart the HALL detection circuit, you need to write the HALLCLR bit in the MASKNXT register to 1, and HALLST restarts the detection circuit from the initial state of 111 to 000.

Hall detection circuitry provides functionality that can be associated with mask autoloading. This feature does not require software intervention to control the output channel waveform of the EPWM.

HallST corresponds to a mask preset cache for each valid state, for a total of 7 mask preset caches:

HALLST(HALLS=1)	The corresponding mask preset cache
000	Mask preset cache7
001	Mask preset cache 1
010	Mask preset cache 2
011	Mask preset cache 3
100	Mask preset cache 4
101	Mask preset cache 5
110	Mask preset cache 6
111	Mask preset cache7
HALLS=0	Mask preset cache 0

If the mask automatically loads presets is enabled, the data in the corresponding mask preset cache will be loaded into the MASK registers in the corresponding state and at the selected load point. For example:

When the position state in HALLST changes from 000 to 001, the data of the mask preset cache 1 is loaded into the MATRIX register at the first loading point when the 001 state is entered.

Later, when the position state in HALLST changes from 001 to 101, the data from mask preset cache 5 is loaded into the MASK register at the first load point of entering the 101 state.

If an incorrect sequence occurs, such as when the CAP2-CAP0 input is changed from 101 to 010, which is not the correct sequence, the position state in HALLST is changed from 101 to 111, and the interrupt flag bit HALLIF is placed at 1. At the first load point of entering the 111 state, the data of the mask preset cache 7 is loaded into the MASK register.

Initially, the data cached by mask preset 7 is loaded into the MASK register at the load point.

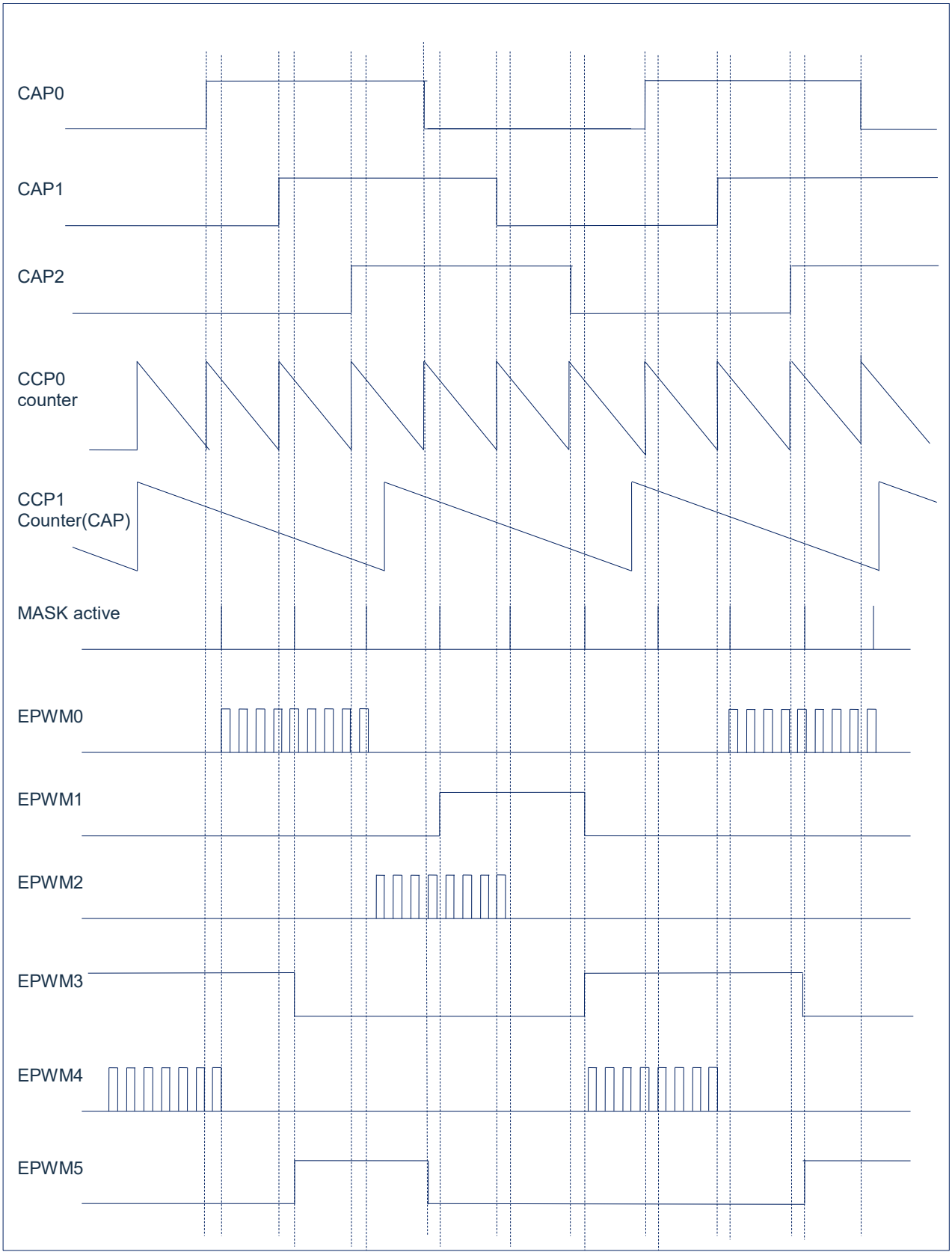


Figure 16-1 1: Hall detection timing example (not representing the actual running waveform).

16.3.14 Brake function

EPWM supports faulty braking. BKODn controls the brake thresholds for 6 channels. The brake function is controlled by the BRKCTL registers.

EPWM brake trigger sources are:

- Simulates the event of Comparator 0
- Simulates the event of Comparator 1
- ADC0 results Comparator 0 event
- ADC1 Result Comparator 0 event
- External high/low level brake signal
- Software brake signal

The brake condition reset also automatically generates a BRKIF flag, and the user can enable the relevant brake break to decide when to cause a brake break.

Note: When a brake event occurs, the EPWM0-EPWM5 count enable bit is cleared by the hardware. The user must first clear the brake event marker and re-enable the EPWMn related channel.

16.3.15 Output channel remapping capability

The output channel remapping capability meets the needs of more flexible typography in applications. The pins of EPWM0-EPWM5 in the chip pin distribution chart default to the corresponding PWM channel output. The desired channel can also be reconfigured with the output channel remapping function.

The default internal channels of EPWM0-EPWM5 are IPG0-IPG5, and any channel of IPG0-IPG5 can be redistributed to EPWMn (n=0-5) through the EPWM output channel remap register POREMAP. The output channel remapping feature only reassigns the port output channels, and its internal controls and interrupts are not remapped.

16.3.16 EPWM configuration process

1) Writing 0x55 lock registers enable EPWM register operations
2) Configure the EPWM clock divider to set the prescale ratio and independent crossover ratio
3) Select Mode, Standalone Mode, or Complementary Mode
4) Set the EPWM period and duty cycle
5) Sets the EPWM output polarity
6) Enables the EPWM counter
7) Configure the relevant IO port as the EPWM function port
8) Enables the associated EPWM channel output
9) 0x00 the LOCK register is written, avoid misoperation of the EPWM-related register until the next time the EPWM-related register needs to be operated

16.3.17 interrupt

The EPWM unit has eight interrupt sources:

- ZIFn—Interrupt flag generated when the EPWM counter counts to zero
- UIFn—The EPWM counter counts up to the CMPDATn interrupt flag
- PIFn—The EPWM counter edges align the count interrupt flags and the center aligns the count interrupt flags
- DIFn—The EPWM counter counts down to the CMPDATn/CMPDDATn interrupt flag
- The DC0IF—EPWM counter counts to an interrupt flag equal to CMPTGD0
- The DC1IF—EPWM counter counts to an interrupt flag equal to CMPTGD1
- HALLIF—Hall status error interrupt flag bit
- BRKIF—Brake interrupt flag

All interrupt flags are hardware-set and must be cleared by software.

16.4 Register mapping

(EPWM Base Address = 0x4A80_0000)

RO: read-only, WO: write-only, R/W: read-write

register	Offset	R/W	description	Reset value
CLKPSC(P1B)	0x000	R/W	EPWM prescaler registers	0x0
CLKDIV(P1B)	0x004	R/W	EPWM clock selection register	0x0
CON(P1B)	0x008	R/W	EPWM control registers	0x0
CON2(P1B)	0x00C	R/W	EPWM control register 2	0x0
CON3(P1B)	0x010	R/W	EPWM control register 3	0x0
PERIOD0(P1A)	0x014	R/W	EPWM cycle register 0	0x0
PERIOD1(P1A)	0x018	R/W	EPWM cycle register 1	0x0
PERIOD2(P1A)	0x01C	R/W	EPWM cycle register 2	0x0
PERIOD3(P1A)	0x020	R/W	EPWM cycle register 3	0x0
PERIOD4(P1A)	0x024	R/W	EPWM cycle register 4	0x0
PERIOD5(P1A)	0x028	R/W	EPWM cycle register 5	0x0
CMPDAT0(P1A)	0x02C	R/W	EPWM comparison register 0	0x0
CMPDAT1(P1A)	0x030	R/W	EPWM comparison register 1	0x0
CMPDAT2(P1A)	0x034	R/W	EPWM comparison register 2	0x0
CMPDAT3(P1A)	0x038	R/W	EPWM comparison register 3	0x0
CMPDAT4(P1A)	0x03C	R/W	EPWM comparison register 4	0x0
CMPDAT5(P1A)	0x040	R/W	EPWM comparison register 5	0x0
POREMAP(P1B)	0x044	R/W	EPWM output channel remap register	0x543210
POEN(P1B)	0x048	R/W	EPWM output control register	0x0
BRKCTL(P1B)	0x04C	R/W	EPWM fail-safe control register	0x0
DTCTL(P1B)	0x050	R/W	EPWM dead-zone length register	0x0
MASK(P1B)	0x054	R/W	EPWM output mask register	0x0
MASKNXT(P1B)	0x058	R/W	EPWM output mask preset register	0x0
CMPTGD0(P1B)	0x05c	R/W	EPWM counter comparison register 0	0x0
CMPTGD1(P1B)	0x060	R/W	EPWM counter comparison register 1	0x0
IMSC(P1B)	0x064	R/W	EPWM interrupt enable register	0x0
RICE	0x068	RO	EPWM interrupt source status register	0x0
PUT	0x06c	RO	EpWM enabled Interrupt status register	0x0
ICLR	0x070	WO	EPWM interrupt clear register	0x0
IFA(P1B)	0x074	R/W	EPWM interrupt accumulate control register	0x0
LOCK	0x078	R/W	EPWM write enable control register	0x0

Note:

1) (P1A/P1B) The registers marked are protected registers.

2) (P1A): When LOCK=55H or AAH, the marked register allows writing; = Other values, forbidden to write.

3) (P1B): When LOCK=55H, the labeled register is allowed to write; = Other values, forbidden to write.

16.5 Register description

16.5.1 EPWM Prescale Register (CLKPSC)

bit	symbol	description	Reset value
31:24	-	Reserved	-
23:16	CLKPSC45	EPWM counters 4 and 5 clock prescale CLK_PSC45 = PCLK/(CLKPSC45+1) If the CLKPSC45=0, the prescaler has no clock output, and the CLKDIVn bit does not work if the clock associated with the PSC is selected	0x0
15:8	CLKPSC23	EPWM counters 2 and 3 clock prescalers CLK_PSC23 = PCLK/(CLKPSC23+1) If the CLKPSC23=0 and the prescaler have no clock output, the COUNTER does not work if the CLKDIVn bit selects a clock associated with the PSC	0x0
7:0	CLKPSC01	EPWM counter 0 and 1 clock prescaler CLK_PSC01 = PCLK/(CLKPSC01+1) If the CLKPSC01=0, the prescaler has no clock output, and the CLKDIVn bit does not work if the PSC-related clock is selected	0x0

16.5.2 EPWM Clock Selection Register (CLKDIV)

bit	symbol	description	Reset value
31:23	-	Reserved	-
22:20	CLKDIV5	Counter 5 clock divider selection 000: CLK_PSC45/2 001: CLK_PSC45/4 010: CLK_PSC45/8 011: CLK_PSC45/16 100: CLK_PSC45/1 Other values: PCLK	0x0
19	-	Reserved	-
18:16	CLKDIV4	Counter 4 clock divider selection 000: CLK_PSC45/2 001: CLK_PSC45/4 010: CLK_PSC45/8 011: CLK_PSC45/16 100: CLK_PSC45/1 Other values: PCLK	0x0
15	-	Reserved	-
14:12	CLKDIV3	Counter 3 clock divider selection 000: CLK_PSC23/2 001: CLK_PSC23/4 010: CLK_PSC23/8 011: CLK_PSC23/16 100: CLK_PSC23/1 Other values: PCLK	0x0
11	-	Reserved	-
10:8	CLKDIV2	Counter 2 clock divider selection 000: CLK_PSC23/2 001: CLK_PSC23/4 010: CLK_PSC23/8	0x0

		011: CLK_PSC23/16 100: CLK_PSC23/1 Other values: PCLK	
7	-	Reserved	-
6:4	CLKDIV1	Counter 1 clock divider selection 000: CLK_PSC01/2 001: CLK_PSC01/4 010: CLK_PSC01/8 011: CLK_PSC01/16 100: CLK_PSC01/1 Other values: PCLK	0x0
3	-	Reserved	-
2:0	CLKDIV0	Counter 0 clock divider selection 000: CLK_PSC01/2 001: CLK_PSC01/4 010: CLK_PSC01/8 011: CLK_PSC01/16 100: CLK_PSC01/1 Other values: PCLK	0x0

16.5.3 EPWM Control Register (CON)

bit	symbol	description	Reset value
31:26	-	Reserved	-
25:24	MODE	EPWM operating mode selection 00: Standalone mode 01: Complementary model 10: Synchronous mode 11: Reserved	0x0
23	GROUNPEN	EPWM grouping function enable bits 0: All PWM channels are independent of each other 1: EPWM0 controls EPWM2, EPWM4, EPWM1 controls EPWM3, EPWM5	0x0
22	ASYMEN	Asymmetric count enablement in EPWM center alignment 1: Symmetry count enables 0: Asymmetric count enablement	0x0
21	CNTTYPE	EPWM count alignment is selected 0: Edge alignment 1: Center alignment	0x0
20	HALT	Counter control bit when DEBUGGING 0: The counter counts normally when halting 1: The counter stops when halting	0x0
19	-	Reserved	-
18	EN_DT45	EPWM counters 4 and 5 dead-zone enable bits 0: Disable counters 4 and 5 dead zones 1: Enable counters 4 and 5 dead zones	0x0
17	EN_DT23	EPWM counters 2 and 3 dead-zone enable bits 0: Disable counters 2 and 3 dead zones	0x0

		1: Enable counters 2 and 3 dead zones	
16	EN_DT01	EPWM counter 0 and 1 dead-zone enable bits 0: Disable counters 0 and 1 dead zones 1: Enable counters 0 and 1 dead bands	0x0
15:14	-	Reserved	-
13	PINV5	EPWM5 output polarity control bit 0: Normal output 1: Inverting output	0x0
12	PINV4	EPWM4 output polarity control bits 0: Normal output 1: Inverting output	0x0
11	PINV3	EPWM3 output polarity control bit 0: Normal output 1: Inverting output	0x0
10	PINV2	EPWM2 output polarity control bit 0: Normal output 1: Inverting output	0x0
9	PINV1	EPWM1 output polarity control bit 0: Normal output 1: Inverting output	0x0
8	PINV0	EPWM0 output polarity control bit 0: Normal output 1: Inverting output	0x0
7:6	-	Reserved	-
5	CNTMODE5	EPWM5 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0
4	CNTMODE4	EPWM4 auto load/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0
3	CNTMODE3	EPWM3 auto load/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0
2	CNTMODE2	EPWM2 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0
1	CNTMODE1	EPWM1 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0
0	CNTMODE0	EPWM0 autoload/single-shot mode 0: Single-shot mode 1: Auto load mode	0x0

16.5.4 EPWM control register (CON2)

bit	symbol	description	Reset value
31:6	-	Reserved	-
5	CNTEN5	EPWM5 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0x0
4	CNTEN4	EPWM4 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0x0
3	CNTEN3	EPWM3 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0x0
2	CNTEN2	EPWM2 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0x0
1	CNTEN1	EPWM1 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0x0
0	CNTEN0	EPWM0 counter enable bit 0: Disable 1: Enable (The bit is cleared automatically after single-pass mode is completed).	0x0

16.5.5 EPWM control register (CON3)

bit	symbol	description	Reset value
31:28	-	Reserved	-
27:26	LOADTYP5	EPWM5 load/interrupt mode selection bits 00: Each zero and period point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next cycle point to load and produce an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0x0
25:24	LOADTYP4	EPWM4 load/interrupt mode select bits 00: Each zero and period point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next cycle point to load and produce an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0x0
23:22	LOADTYP3	EPWM3 load/interrupt mode selection 00: Each zero and period point loads and produces an interrupt flag 01: The first zero point alternates with the next cycle point to load and produce an interrupt flag 10: Each zero point is loaded with an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0x0
21:20	LOADTYP2	EPWM2 load/interrupt mode selection 00: Each zero and period point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next cycle point to load and produce an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0x0
19:18	LOADTYP1	EPWM1 load/interrupt mode selection bits 00: Each zero and period point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next cycle point to load and produce an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0x0
17:16	LOADTYP0	EPWM0 load/interrupt mode selection 00: Each zero and period point loads and produces an interrupt flag 01: Each zero point is loaded with an interrupt flag 10: The first zero point alternates with the next cycle point to load and produce an interrupt flag 11: Every two zeros are loaded with an interrupt flag	0x0

15:14	-	Reserved	-
13	LOADEN5	EPWM 5-cycle/comparator load enable 0: Disable 1: Enable (hardware is automatically cleared to zero after loading)	0x0
12	LOADEN4	EPWM4 cycle/comparator loading enable bit 0: Disable 1: Enable (hardware is automatically cleared to zero after loading)	0x0
11	LOADEN3	EPWM3 cycle/comparator loading enable bit 0: Disable 1: Enable (hardware is automatically cleared to zero after loading)	0x0
10	LOADEN2	EPWM2 cycle/comparator loading enable bit 0: Disable 1: Enable (hardware is automatically cleared to zero after loading)	0x0
9	LOADEN1	EPWM1 cycle/comparator loading enable bit 0: Disable 1: Enable (hardware is automatically cleared to zero after loading)	0x0
8	LOADEN0	EPWM0 cycle/comparator loading enable bits 0: Disable 1: Enable (hardware is automatically cleared to zero after loading)	0x0
7:6	-	Reserved	-
5	CNTCLR5	The EPWM5 counter clears the zero position 0: Disable 1: Enable (hardware auto-zero)	0x0
4	CNTCLR4	The EPWM4 counter clears the zero position 0: Disable 1: Enable (hardware auto-zero)	0x0
3	CNTCLR3	The EPWM3 counter is cleared to zero 0: Disable 1: Enable (hardware auto-zero)	0x0
2	CNTCLR2	The EPWM2 counter clears the zero bit 0: Disable 1: Enable (hardware auto-zero)	0x0
1	CNTCLR1	The EPWM1 counter clears the zero bit 0: Disable 1: Enable (hardware auto-zero)	0x0
0	CNTCLR0	The EPWM0 counter clears the zero bit 0: Disable 1: Enable (hardware auto-zero)	0x0

16.5.6 EPWM period register 0-5 (PERIOD0-5)

bit	symbol	description	Reset value
31:16	-	Reserved	-
15:0	PERIODn	EPWMn counter period value	0x0

16.5.7 EPWM comparision registers 0-5 (CMPDAT0-5)

bit	symbol	description	Reset value
31:16	CMPDDATn	The EPWMn counter compares values downwards	0x0
15:0	CMPDATn	EPWMn counter comparison values	0x0

16.5.8 EPWM output control register (POEN)

bit	symbol	description	Reset value
31:12	-	Reserved	-
11	MASKLE	EPWM mask control preset data loading enable bit 0: Disable 1: Enable (Allows the data of the MASKNXT register to be loaded into the MASK register, and prohibits writing to the MASK register. In addition, when this bit is 1, the mask data will not be loaded immediately, and will not be loaded until the corresponding loading point is reached.)	0
10:8	MASKLS	EPWM mask control data loading time selection bit 000: Load at EPWM0 load point 001: Load at EPWM1 load point 010: Load at EPWM2 load point 011: Load at EPWM3 load point 100: Load at EPWM4 load point 101: Load at EPWM5 load point 11x: Reserved	0
7:6	-	Reserved	-
5:0	POENn	EPWMn output enable bit 0: EPWM channel n output inhibit 1: EPWM channel n output enable	0

16.5.9 EPWM Output Channel Remap Register (POREMAP)

bit	symbol	description	Reset value
31:24	PWMRMEN	The EPWM channel remap function enables control AAH: The remap function is enabled EPWMn Which channel output is chosen by PWMnRM Other: The remapping feature is prohibited The EPWMn fixed channel outputs are as follows: EPWM0<- IPG0 EPWM1<- IPG1 EPWM2<- IPG2 EPWM3<- IPG3 EPWM4<- IPG4 EPWM5<- IPG5	0x0
23	-	Reserved	-
22:20	PWM5RM	EPWM channel 5 remap selection bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: Reserved	0x5
19	-	Reserved	-
18:16	PWM4RM	EPWM channel 4 remap selection bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: Reserved	0x4
15	-	Reserved	-
14:12	PWM3RM	EPWM channel 3 remap select bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: Reserved	0x3
11	-	Reserved	-
10:8	PWM2RM	EPWM channel 2 remap select bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: Reserved	0x2
7	-	Reserved	-
6:4	PWM1RM	EPWM channel 1 remap selects bits	0x1

		000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: Reserved	
3	-	Reserved	-
2:0	PWM0RM	EPWM channel 0 remap select bits 000: Map the output of IPG0 001: Map the output of IPG1 010: Map the output of IPG2 011: Map the output of IPG3 100: Map the output of IPG4 101: Map the output of IPG5 11x: Reserved	0x0

16.5.10 EPWM Fail-Safe Control Register (BRKCTL)

bit	symbol	description	Reset value
31	BRKEN	EPWM brake function always enables the bit 0: Disable 1: Enable	0x0
30:20	-	Reserved	-
19	ACMP1BKEN	Analog comparator 1 outputs brake enable bits 0: Disable 1: Enable (allow ACMP1 comparison event to trigger braking)	0x0
18	ACMP0BKEN	Analog comparator 0 output brake enable bit 0: Disable 1: Enable (allows ACMP0 comparison events to trigger braking)	0x0
17	-	Reserved	-
16	ADC1MP0BKEN	ADC1 comparator 0 output brake enable bit 0: Disable 1: Enable	0x0
15:13	-	Reserved	-
12	SWBRK	Software brake enable bit 0: Software brakes are prohibited 1: Immediately generate software brakes	0x0
11	EXTBRKEE	External hardware brake edges detect enable levels 0: Disable 1: Enable	0x0
10	EXTBRKES	External hardware brake edges detect selected bits 0: The descending edge triggers the brakes 1: The rising edge triggers the brakes	0x0
9	EXTBRKLE	External hardware brake level detection enable bit 0: Disable 1: Enable	0x0
8	EXTBRKLS	External hardware brake level detection select bit 0: Low levels produce brakes 1: High levels produce brakes	0x0
7:6	-	Reserved	-
5:0	BRKODn	EPWMn brake output level select bit 0: When the brakes fail, channel n outputs a low level 1: When the brakes fail, channel n outputs high	0x0

16.5.11 EPWM Dead Zone Length Register (DTCTL)

bit	symbol	description	Reset value
31:30	-	Reserved	-
29:20	DTI45	Channel 4 and Channel 5 dead-zone length registers Dead-zone = PWM_CLK45×DTI45	0x0
19:10	DTI23	Channel 2 and Channel 3 dead-zone length registers Dead-zone = PWM_CLK23×DTI23	0x0
9:0	DTI01	Channel 0 and channel 1 dead-zone length registers Dead-zone = PWM_CLK01× DTI01	0x0

16.5.12 EPWM Mask Output Control Register (MASK)

bit	symbol	description	Reset value
31:14	-	Reserved	-
13	MASKEN5	EPWM5 mask output enable bits 0: Disable 1: Enable	0x0
12	MASKEN4	EPWM4 mask output enable bits 0: Disable 1: Enable	0x0
11	MASKEN3	EPWM3 mask output enable bits 0: Disable 1: Enable	0x0
10	MASKEN2	EPWM2 mask output enable bits 0: Disable 1: Enable	0x0
9	MASKEN1	EPWM1 mask output enable bits 0: Disable 1: Enable	0x0
8	MASKEN0	EPWM0 mask output enable bits 0: Disable 1: Enable	0x0
7:6	-	Reserved	-
5	MASKD5	EPWM5 mask data 0: Output 0 1: Output 1	0x0
4	MASKD4	EPWM4 mask data 0: Output 0 1: Output 1	0x0
3	MASKD3	EPWM3 mask data 0: Output 0 1: Output 1	0x0
2	MASKD2	EPWM2 mask data 0: Output 0 1: Output 1	0x0
1	MASKD1	EPWM1 mask data 0: Output 0 1: Output 1	0x0
0	MASKD0	EPWM0 mask data 0: Output 0 1: Output 1	0x0

16.5.13 EPWM Mask Output Control Preset Register (MASKNXT)

bit	symbol	description	Reset value
31:25	-	Reserved	-
24	HALLS	HALL detect mode enable bit 0: Disable 1: Enable	0x0
23	HALLCLR	HALL error status clear bit 0: Writing 0 is invalid 1: Write 1 to clear the error state of HALLST and return it to the initial state of 000. Read as 0. NOTE 1: If the error status or sequence occurs, HALLST=111, the HALL detection function stops. When the HALL status is enabled again, you need to write 1 to clear the status of 111.	0x0
22:20	HALLST	Status bits of hall interface (read-only) Detects the status corresponding to {CAP2, CAP1, CAP0} 000: Status is 0 (initial state) 001: The status is 1 010: The status is 2 011: The status is 3 100: The status is 4 101: The status is 5 110: The status is 6 111: Error status Note 1: This state is the status of the HALL interface detected inside the chip, which can be used to determine whether it has entered a valid state, if the status of the three HALL sensors is wrong or the order of the states is wrong, the status bit is 111. Valid Sequence 1: … 6-2-3-1-5-4-6-… Valid Sequence 2: … 6-4-5-1-3-2-6-… NOTE 2: In a valid status bit, if the mask preset data loading function is enabled, the corresponding mask preset cache data is loaded into the MASK register at the loading point. For example, after hall detection changes to state 3, the first loading point after entering state 3 loads the data of mask preset cache 3 into the MASK register. NOTE 3: Output data from mask cache 7 in initial state 000 or error state 111.	0x0
19	-	Reserved	-
18:16	PMASKSEL	Mask preset cache selection bits; 000: Select mask preset cache 0 001: Select Mask Preset Cache1 010: Select Mask Preset Cache 2 011: Select Mask Preset Cache3 100: Select Mask Preset Cache4 101: Select Mask Preset Cache5 110: Select Mask Preset Cache6 111: Select Mask Preset Cache7 Note 1: This selection bit affects the reading and writing of data in the lower 16 bits, and there are 6 mask preset caches inside the EPWM	0x0

		If 000: The register reads and writes data as low as 16 bits for the mask cache 0. If 001: The register reads and writes data as low as 16 bits for the mask cache 1. If 110: The register reads and writes data in cache 6 as low as 16 bits. Note 2: When HALLEN=0, the default loading mask preset cache is 0.	
15:14	-	Reserved	-
13	PMASKEN5	The EPWM5 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
12	PMASKEN4	The EPWM4 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
11	PMASKEN3	The EPWM3 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
10	PMASKEN2	The EPWM2 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
9	PMASKEN1	The EPWM1 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
8	PMASKEN0	The EPWM0 mask output enables preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
7:6	-	Reserved	-
5	PMASKD5	EPWM5 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
4	PMASKD4	EPWM4 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
3	PMASKD3	EPWM3 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
2	PMASKD2	EPWM2 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
1	PMASKD1	EPWM1 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0
0	PMASKD0	EPWM0 mask data preset bits (This bit can be set at the load point of EPWMn to load into the MASK register)	0x0

16.5.14 EPWM Trigger Comparison Register (CMPTGD0-1)

bit	symbol	description	Reset value
31:20	-	Reserved	-
19	CMPTGDSn	EPWM count comparator n trigger mode (In effect under Center Alignment Count) 0: Triggered when counting down 1: Triggered when counting up	0x0
18:16	CMPPCHSn	EPWM digital comparator n comparison channel selection 000: Counter of PWM0 001: Counter of PWM1 010: Counter of PWM2 011: Counter of PWM3 100: Counter of PWM4 101: Counter of PWM5 Other values: Counter of PWM0	0x0
15:0	CMPTGDn	EPWM count comparator n triggers the comparison value	0x0

16.5.15 EPWM Interrupt Enable Register (IMSC)

bit	symbol	description	Reset value
31	EN_BRKIF	EPWM brake interrupt enable bit 0: Disable 1: Enable	0x0
30	EN_HALLIF	HALL status Error interrupt enable bit 0: Disable 1: Enable	0x0
29:24 n=5-0	EN_DIFn	EPWMn down comparision interrupt enable bit 0: Disable 1: Enable	0x0
23:22	-	Reserved	-
21:16 n=5-0	EN_UIFn	EPWMn up comparision interrupt enable bits 0: Disable 1: Enable	0x0
15	EN_DC1IF	Count comparator 1 interrupt enable bit 0: Disable 1: Enable	0x0
14	EN_DC0IF	Count comparator 0 interrupt enable bit 0: Disable 1: Enable	0x0
13:8 n=5-0	EN_PIFn	EPWMn cycle interrupt enable bit 0: Disable 1: Enable	0x0
7:6	-	Reserved	-
5:0 n=5-0	EN_ZIFn	EPWMn zero-point interrupt enable bit 0: Disable 1: Enable	0x0

16.5.16 EPWM Interrupt Source Status Register (RIS)

bit	symbol	description	Reset value
31	RIS_BRKIF	EPWM brake interrupt source status bit 0: No interrupt was generated 1: An interrupt has been generated	0x0
30	RIS_HALLIF	HALL Status Error Interrupt Source Status Bit 0: No interrupt was generated 1: An interrupt has been generated	0x0
29:24 n=5-0	RIS_DIFn	EPWMn compares the interrupt source status bits downwards 0: No interrupt was generated 1: An interrupt has been generated	0x0
23:22	-	-	-
21:16 n=5-0	RIS_UIFn	EPWMn compares interrupt source status bits upwards 0: No interrupt was generated 1: An interrupt has been generated	0x0
15	RIS_DC1IF	Count comparer 1 interrupt status bit 0: Disable 1: Enable	0x0
14	RIS_DC0IF	Count comparer 0 interrupt status bits 0: Disable 1: Enable	0x0
13:8 n=5-0	RIS_PIFn	EPWMn cycle interrupt source status bits 0: No interrupt was generated 1: An interrupt has been generated	0x0
7:6	-	-	-
5:0 n=5-0	RIS_ZIFn	EPWMn zero-point interrupt source status bit 0: No interrupt was generated 1: An interrupt has been generated	0x0

16.5.17 EPWM Enabled Interrupt Status Register (MIS)

bit	symbol	description	Reset value
31	MIS_BRKIF	The EPWM brake enabled Interrupt status bit 0: No interrupt was generated 1: Enabled and produced an interrupt	0x0
30	MIS_HALLIF	HALL status error enabled Interrupt status bit 0: No interrupt was generated 1: Enabled and produced an interrupt	0x0
29:24 n=0-5	MIS_DIFn	EPWMn down comparision enabled interrupt status bit 0: No interrupt was generated 1: Enabled and produced an interrupt	0x0
23:22	-	Reserved	-
21:16 n=0-5	MIS_UIFn	EPWMn up comparison enabled interrupt status bits 0: No interrupt was generated 1: Enabled and produced an interrupt	0x0
15	RIS_DC1IF	Count Comparer 1 enabled Interrupt status bit 0: Disable 1: Enable	0x0
14	RIS_DC0IF	Count comparator 0 enabled Interrupt status bit 0: Disable 1: Enable	0x0
13:8 n=0-5	MIS_PIFn	The EPWMn period enabled Interrupt status bit 0: No interrupt was generated 1: Enabled and produced an interrupt	0x0
7:6	-	Reserved	-
5:0 n=0-5	MIS_ZIFn	The EPWMn zero point enabled Interrupt status bit 0: No interrupt was generated 1: Enabled and produced an interrupt	0x0

16.5.18 EPWM Interrupt Clear Control Register (ICLR)

bit	symbol	description	Reset value
31	ICLR_BRKIF	EPWM brake interrupt clear control position Write 0: Does not affect Write 1: Clear the RIS_BRKIF flag bits	0x0
30	ICLR_HALLIF	HALL status error interrupt clear control bit Write 0: Does not affect Write 1: Clear ICLR_HALLIF flag bit	0x0
29:24 n=0-5	ICLR_DIFn	EPWMn down comparision the interrupt clear control bit Write 0: Does not affect Write 1: Clear RIS_DIFn flag bits	0x0
23:22	-	Reserved	-
21:16 n=0-5	ICLR_UIFn	EPWMn up comparision interrupt clear control bit Write 0: Does not affect Write 1: Clear RIS_UIFn flag bits	0x0
15	ICLR_DC1IF	Count comparator 1 interrupt clear control bit Write 0: Does not affect Write 1: Clear RIS_DC1IF flag bits	0x0
14	ICLR_DC0IF	Count comparator 0 interrupt clear control bits Write 0: Does not affect Write 1: Clear the RIS_DC0IF flag bit	0x0
13:8 n=0-5	ICLR_PIFn	EpWMn cycle interrupts the clear control bit Write 0: Does not affect Write 1: Clear the RIS_PIFn flag bit	0x0
7:6	-	Reserved	-
5:0 n=0-5	ICLR_ZIFn	EPWMn zero-point interrupt clear control bit Write 0: Does not affect Write 1: Clear RIS_ZIFn flag bits	0x0

16.5.19 EPWM Interrupt Accumulation Control Register (IFA)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:4	ZIFCMP	Zero-point interrupt accumulates the comparison value When ZIFn interrupts accumulate to (IFCMP+1), ZIFn corresponds to interrupt flag bit set to 1	0x0
3:1	-	Reserved	-
0	ZIFAEN	Zero-point interrupt accumulate enable bits 0: Disable 1: Enable	0x0

16.5.20 EPWM Write Enable Control Register (LOCK)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	LOCK	When LOCK=0x55, enable the operation of the EPWM other registers; When LOCK=0xAA, only the EPWM cycle register and the comparison register are enabled; When LOCK=other values, operation of EPWM-related registers is prohibited.	0x0

17. Universal asynchronous transceiver (UART0/1)

17.1 overview

Includes 2 universal asynchronous serial interfaces, supports hardware flow control, software flow control, and supports 16-byte transmit and receive FIFOs.

17.2 characteristic

- Full-duplex, asynchronous communication.
- Independent 16 bytes to send/receive FIFOs.
- Support hardware automatic flow control (CTS, RTS).
- Support software flow control function (XOFF, XON).
- Optional Receive cache trigger level.
- Programmable serial interface features.
  - The data bit length can be set to 5 to 8 bits.
  - The check digits can be set to be parity, no check, or fixed check bits for generation and detection.
  - The stop bit length can be set to 1 bit, 1.5 bits, or 2 bits.

17.3 Feature description

17.3.1 UART function mode

UART is a full-duplex asynchronous communication interface. The UART transceiver each contains a 16-byte FIFO buffer, and the user can set the receive cache trigger level, and can flexibly set the transmit byte length and stop bit length.

Support hardware automatic flow control function (CTS, RTS), and the trigger level of RTS flow control can be set, and the communication parameters of the full-duplex serial interface can be set.

17.3.2 UART interrupts and status

UART supports 9 types of interrupts, including the following:

- Receive interrupts after the threshold level reaches.
- Send a FIFO empty interrupt.
- Line state interrupt (parity error, frame error, interruption interrupt).
- Modem status interrupt.
- Receive buffer timing overflow interrupt.
- Hardware flow interrupt (CTS/RTS).
- Software flow interrupt.

17.4 Register mapping

(UART0 base address = 0x4480_0000; UART1 base address = 0x4500_0000).

RO: read-only; WO: Write only; R/W: Read and write

The x values in the following registers are 0-1.

register	Offset	R/W	description	Reset value
RBR	0x000	RO	Receive cache register	-
THR	0x004	WO	Send cache register	-
DLR	0x008	R/W	Baud rate divider register	0x01
I	0x00c	R/W	Interrupt enable register	0x0
IIR	0x010	RO	Interrupt status register	0x01
FCR	0x014	WO	FIFO control register	0x0
LCR	0x018	R/W	Line control register	0x0
MCR	0x01C	R/W	Modem control register	0x0
LSR	0x020	RO	Line status register	0x60
MSR	0x024	RO	Modem status register	0x0
SCR	0x028	R/W	Cache register	0x0
EFR	0x02C	R/W	Advanced settings register	0x0
XON1	0x030	R/W	XON1 register	0x0
XON2	0x034	R/W	XON2 register	0x0
XOFF1	0x038	R/W	XOFF1 register	0x0
XOFF2	0x03C	R/W	XOFF2 register	0x0

17.5 Register description

17.5.1 Receive Cache Register (RBR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	RBR	A read operation that returns the received data from the FIFO area	-

17.5.2 Send Cache Register (THR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	THR	Writing data to the send buffer, the UART module will send the data at the front end of the FIFO in turn	-

17.5.3 Baud rate divider register (DLR)

bit	symbol	description	Reset value
31:16	-	Reserved	-
15:0	DLR	Baud rate = PCLK/16DLR×	0x1

17.5.4 Interrupt enable register (IER)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7	CTSIE	CTS interrupt enable bit (requires AUTOIEN=1 to write). 0: Disable 1: Enable	0x0
6	RTSIE	RTS interrupt enable bit (requires AUTOIEN=1 to write). 0: Disable 1: Enable	0x0
5	XOFIE	XOFF interrupt enable bit (requires AUTOIEN=1 to write). 0: Disable 1: Enable	0x0
4	-	Reserved	-
3	MDSIE	Modem status interrupt enable bit 0: Disable 1: Enable	0x0
2	RLSIE	Receive line status interrupt enable bit 0: Disable 1: Enable	0x0
1	THREIE	Sends hold register null interrupt enable bit 0: Disable 1: Enable	0x0
0	RBRIE	Receive data valid interrupt/receive timer overflow interrupt enable bit 0: Disable 1: Enable	0x00

17.5.5 Interrupt Status Register (IIR)

bit	symbol	description	Reset value
31:6	-	Reserved	-
5	INTHFC	Hardware flow control status If the bit is 1, a rising edge is detected at the RTS or CTS pin and can be cleared by reading UARTxIIR	0x0
4	INTSFC	Software flow control status If the bit is 1, an XOFF character was received. This bit can be cleared by reading the UARTxIIR	0x0
3:1	INTID	Interrupt status indication 0x0: Modem state changes 0x1: The send hold register is empty 0x2: The received data is valid 0x3: Line status received 0x6: Receive timer overflow	0x0
0	INT STATUS	Interrupt status 0: At least one interrupt is in the queue 1: There is no interrupt in the queue	1

17.5.6 FIFO Control Register (FCR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:6	RXTL	Receive trigger level, which indicates how many bytes were received before the interrupt was triggered 0x0: Level 0 (1 byte). 0x1: Level 1 (4 bytes). 0x2: Level 2 (8 bytes). 0x3: Level 3 (14 bytes).	0x0
5:4	TXTL	Send trigger level, which indicates how many bytes were sent to trigger an interrupt (AutoIEN=1 is required to write). 0x0: Level 0 (N-1 bytes, N> = 1 is required, otherwise no interrupt will occur). 0x1: Level 1 (N-4 bytes, N> = 4 is required, otherwise there is no interrupt). 0x2: Level 2 (N-8 bytes, N> = 8 is required, otherwise no interrupt is generated). 0x3: Level 3 (N-14 bytes, N> = 14 is required, otherwise no interrupt is generated). Note: N is the number of bytes written to the FIFO, N< = 17.	0x0
3	-	Reserved	-
2	TXFIFO RST	Send a FIFO reset write 0: Does not affect 1: Clears all data in the sending FIFO and resets the FIFO pointer. The bit clears from zero.	0x0
1	RXFIFO RST	Receives a FIFO reset write 0: Does not affect 1: Clears all data in the sending FIFO and resets the FIFO pointer. The bit clears from zero.	0x0
0	FIFOEN	FIFO enable bit 0: FIFO is prohibited 1: Enable FIFO Note: When this bit changes, all data in the sending and receiving FIFOs is automatically cleared	0x0

17.5.7 Line Control Register (LCR)

bit	symbol	description	Reset value
31:7	-	Reserved	-
6	BCON	Break control bit When the bit writes 1 and enables the Break transfer, the TXD port will force the output logic 0	0x0
5:4	PSEL	Parity bit selection 0x0: Odd checksum, where the odd number of logical 1s is sent and detected in each byte 0x1: For parity, an even number of logical 1s is sent and detected in each byte 0x2: The checksum is forced to 1 0x3: The checksum is forced to be 0	0x0
3	PEN	The parity enable bit 0: Checksum generation and detection is prohibited 1: Enables checksum generation and detection	0x0
2	SBS	Stop bit selection 0: 1-bit stop bit 1: The stop bit is 1.5 bits when the send word length is 5 bits, and 2 bits when the send word length is other	0x0
1:0	WLS	The word length selection bit 0x0: 5 digits long 0x1: 6-digit word length 0x2: 7-digit word length 0x3: 8-digit word length	0x0

17.5.8 Modem Control Register (MCR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7	XOFFS	XOFF status bit read only 1: XOFF characters were received 0: XON characters were received	0x0
6	IRENE	IrDA Modem enable bit 0: Disable 1: Enable	0x0
5	-	Reserved	-
4	MLBM	Modem loopback mode 0: Modem loopback mode is disabled 1: Enables Modem loopback mode	0x0
3:2	-	Reserved	-
1	RTS	Modem mode RTS output bits 0: RTS output high 1: RTS output low When modem loopback mode is enabled, the bit is read as 0	0x0
0	-	Reserved	-

17.5.9 Line Status Register (LSR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7	RXFE	Receive FIFO error bits (read-only) This bit set to 1 when a receive frame error occurs, a check error, or an interrupting interrupt occurs When there are no errors in the FIFO queue, the bit can be cleared by reading the LSR register	0x0
6	TEMT	Send cache null flag bit (read-only) 0: The send cache has undelivered data 1: The send cache is empty	1
5	THRE/FIFOE	When FIFOEN=0, it is indicated as a null flag bit (read-only) of the send register 0: The send register has unsent data 1: The send register is empty When FIFOEN=1, it is indicated as sending a FIFO null flag bit (read-only). 0: Sending FIFO has not sent data 1: Send FIFO is empty	1
4	WOULD	Interruption interrupt flag bit (read-only) 0: No interrupt interrupts detected 1: A interrupted interrupt was detected When the UART data input remains low during a transmission (start bit, data, check digit, stop bit), an interruption interrupt is triggered. The UART remains idle until the data input is high. This bit can be cleared by reading the LSR register	0x0
3	FE	Frame error flag bit (read-only) 0: No frame errors were detected 1: A frame error was detected This bit can be cleared by reading the LSR register	0x0
2	ON	Checksum error flag bit (read-only) 0: No checksum errors were detected 1: A checksum error was detected This bit can be cleared by reading the LSR register	0x0
1	OE	FIFO overflow error flag bit (read-only) 0: No FIFO overflow error detected 1: A FIFO overflow error was detected When the FIFO is full and new data is received, a FIFO overflow error occurs, in which case the data in the FIFO is not overwritten, but the newly received data is lost. This bit can be cleared by reading the LSR register	0x0
0	RDR	Receive data valid flag bits (read-only) 0: There is no unread data in the receive area 1: There is unread data in the receive area	0x0

17.5.10 Modem Status Register (MSR)

bit	symbol	description	Reset value
31:5	-	Reserved	-
4	CTS	CTS pin status (read-only) 0: The CTS pin input status is low 1: The CTS pin input status is high When moden loopback mode is enabled, the CTS pin status is connected to the MCR[1].	0x0
3:1	-	Reserved	-
0	DCTS	Detects CTS pin level change marker bits (read-only) 0: There is no level change on the CTS input pins 1: The CTS input pins have level variations This bit can be cleared by reading the MSR register	0x0

17.5.11 Cache register (SCR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	PAD	Read-write 8-bit registers	0x0

17.5.12 Advanced Setup Register (UARTxEFR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7	AUTOCTS	Hardware send flow control 0: Disable 1: Enable	0x0
6	AUTORTS	Hardware receive flow control 0: Disable 1: Enable	0x0
5	-	Reserved	-
4	AUTOIEN	Flow control interrupt enable 0: Disable 1: Enable (Control CTSIE, RTSIE, XOFIE Write Enable)	0x0
3:2	TXSWFC	Send software flow control bit 0x0: Disable sending software flow control 0x1: Send XON2/XOFF2 as stream control characters 0x2: Send XON1/XOFF1 as stream control characters 0x3: Send XON1 & XON2 and XOFF1 & XOFF2 as stream control characters	0x0
1:0	RXSWFC	Receives software flow control bit 0x0: Disable receiving software flow control 0x1: Receive XON2/XOFF2 as stream control characters 0x2: Receive XON1/XOFF1 as stream control characters 0x3: Receive XON1 & XON2 and XOFF1 & XOFF2 as stream control characters	0x0

17.5.13 XON1, XON2 register (XON1/XON2)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	HXON	XON characters	0x0

17.5.14 XOFF1, XOFF2 register (XOFF1/XOFF2)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	HXOFF	XOFF characters	0x0

18. I2C Serial Interface Controller (I2C)

18.1 overview

I2C is a two-wire bidirectional serial bus that provides a simple and efficient connection for data exchange between devices. I2C is a true multi-master bus that incorporates conflict detection and arbitration mechanisms. Conflict detection and arbitration mechanisms are used to prevent data corruption in cases where two or more hosts are simultaneously trying to control the bus.

18.2 Characteristic

- Supports master/slave mode.
- Bidirectional data transfer between master and slave.
- Multi-master bus.
- Simultaneous data arbitration between multiple hosts to avoid serial data corruption on the bus.
- The bus uses a serial synchronous clock that enables different rates between devices.
- Serial synchronous clocks can be used as a handshake mechanism to implement suspend and resume serial transmissions.
- Programmable clocks can be used for a variety of rate controls.
- Supports 7-bit/10-bit slave address modes.
- Supports multi-address recognition (4 groups of slave addresses with mask option).
- Wake-up mode is supported.

18.3 Feature description

18.4 Register mapping

(I2C0 base address = 0x4800_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
CONSET	0x000	R/W	I2C control set register	0x0
CONCLR	0x004	WO	I2C control clear register	0x0
STATE	0x008	RO	I2C status register	0xF8
THAT	0x00C	R/W	I2C data register	0x0
CLK	0x010	R/W	I2C clock control registers	0x0
ADR0	0x014	R/W	I2C Slave address register 0	0x0
ADM0	0x018	R/W	I2C Slave address mask register 0	0xFE
XADR0	0x01C	R/W	I2C extended slave address register 0	0x0
XADM0	0x020	R/W	I2C extended slave address mask register 0	0x1FE
RST	0x024	WO	I2C software reset registers	0x0
ADR1	0x028	R/W	I2C Slave Address Register 1	0x0
ADM1	0x02C	R/W	I2C Slave Address Mask Register 1	0xFE
ADR2	0x030	R/W	I2C Slave Address Register 2	0x0
ADM2	0x034	R/W	I2C Slave Address Mask Register 2	0xFE
ADR3	0x038	R/W	I2C Slave Address Register 3	0x0
ADM3	0x03C	R/W	I2C Slave Address Mask Register 3	0xFE

18.5 Register description

18.5.1 I2C Controls set Register (CONSET)

bit	symbol	description	Reset value
31:9	-	Reserved	-
8	GCF	I2C broadcasts the call flag bit read only 0: The broadcast call was not received 1: Broadcast call address matching The bit is cleared to zero when new data is received or sent	0x0
7	I2CIE	Interrupt enable bit 0: Disable 1: Enable	0x0
6	I2CEN	I2C interface enable bit 0: Disable the I2C interface 1: Enables the I2C interface Note: Enables the I2C interface by writing 1 in the I2CEN bit and disables the I2C interface by writing 1 in the I2CENC bit (I2CxCONCLR).	0x0
5	IS	Startup flag bit Write 1, I2C into host mode and send a start signal; - When I2C is already in host mode, a restart signal is sent. - When I2C is in slave mode, write 1 ends the current transfer and enters master mode while the bus is idle. Writing 0 does not affect. - When the startup bit or restart bit sending is complete, the bit is automatically zeroed.	0x0
4	HUNDRED	Stop flag bit When you write 1 in host mode, a stop bit is sent. When writing 1 in slave mode, the I2C module receives a stop bit as if it were received - When the STA and STO are set at the same time, the I2C module sends a stop bit and then a start bit. - When the stop bit sending is complete, the bit is automatically zeroed.	0x0
3	YES	I2C interrupt flag bit read only When thebus state of I2C changes, this position can be cleared by writing 1 in the SIC bit.	0x0
2	AA	Reply flag bit 0: No ACK signal was received 1: Reply to the ACK signal in the following cases ● When the slave address matches ● Enables broadcast calls and receives broadcast addresses ● When data is received in master or slave mode, the bit can be zeroed by writing 1 in the AAC bit	0x0
1	XADRF	I2C slave 10-bit address flag bit read only 0: The I2C address does not match 1: I2C 10-bit address matches The bit is cleared to zero when new data is sent or received	0x0
0	ADRF	I2C Slave 7-bit address flag bit read only 0: The I2C address does not match	0x0

		1: I2C 7-bit address matches The bit is cleared to zero when new data is sent or received	

18.5.2 I2C Control Clear Register (CONCLR)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7	I2CIEC	I2C Interrupt disable bit Write 1 clear I2CIE bit Writing 0 does not affect	0x0
6	I2CENC	The I2C interface disable bits Write 1 clear I2CEN bit Writing 0 does not affect	0x0
5	STAC	The startup flag clears zero bit Write 1 to zero the STA bit Writing 0 does not affect	0x0
4	-	Reserved	-
3	SIC	TheI2Cinterrupt flag clear zero bit Write 1 clear SI bit Writing 0 does not affect	0x0
2	AAC	The I2C answer flag clear zero bit Write 1 clear zero AA bit Writing 0 does not affect	0x0
1:0	-	Reserved	-

I2C operations require the appropriate flag bits to be cleared to proceed to the next state.

18.5.3 I2C Status Register (STAT)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	Status	I2C status code 00H: Bus error (valid only in host mode) 08H: Startup bit send complete 10H: Restart bit send complete 18H: The address + write bit is sent and the ACK is received 20H: Address + write bit sent completed, ACK was not received 28H: In host mode, the data transmission is complete and the ACK is received 30H: The data transmission in host mode is complete and the ACK is not received 38H: Arbitration fails during address or data transfer 40H: Address + read bit sent completed, ACK received 48H: Address + read bit sent completed, ACK was not received 50H: The data is received in host mode and the ACK is replied to 58H: Data is received in host mode and the ACK is not replied to 60H: Receives the address + write bit in the slave mode and replies to the ACK 68H: Host Arbitration fails, slave address + write bit is received, reply ACK 70H: Receive the broadcast call address, reply to the ACK 78H: Host Arbitration fails, receives broadcast call address, reply ACK 80H: After the slave address matches, the data is received and the ACK is replied 88H: After the slave address matches, the data is received and the ACK is not replied 90H: After receiving the broadcast call address from the slave machine, the data is received and the ACK is replied 98H: After receiving the broadcast call address from the slave, the data is received and the ACK is not replied A0H: Receive a stop signal or restart signal in slave mode A8H: Receives the address + read bit in slave mode and replies to the ACK B0H: The host arbitration fails, the slave address + read bit is received, and the ACK is replied B8H: After sending data from machine mode, the ACK is received C0H: After sending data from machine mode, the ACK was not received C8H: After sending the last data in slave mode, the ACK is received D0H: After sending the last data in slave mode, the ACK was not received D8H: Unused E0H: After sending the second address in host mode, the ACK is received E8H: After sending the second address in host mode, the ACK was not received F0H: Unused F8H: Unknown state Other: Reserved	0xF8

18.5.4 I2C Data Register (DAT)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	Data	Data received or to be sent	0x0

18.5.5 I2C Clock Control Register (CLK)

bit	symbol	description	Reset value
31:7	-	Reserved	-
6:4	M	Sample clock = PCLK/(2^M× (N+1)). SCL clock= PCLK/（2^M×（N+1）×10）	0x0
3:0	N		0x0

18.5.6 I2C Slave address register (ADR0/ADR1/ADR2/ADR3)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:1	Address	Slave address	0x0
0	GC	1: Enables broadcast call address recognition 0: Disable broadcast call address recognition	0x0

18.5.7 I2C Slave address mask register (ADM0/ADM1/ADM2/ADM3)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:1	MASK	Mask bits 0: The bit address is not compared 1: Compare the bit address	0x7F
0	-	Reserved	-

18.5.8 I2C Extends the Slave Address Register (XADR0)

bit	symbol	description	Reset value
31:11	-	Reserved	-
10:1	Address	10-bit slave address	0x0
0	GC	1: Enables broadcast call address recognition 0: Disable broadcast call address recognition	0x0

18.5.9 I2C Extended Slave Address Mask Register (XADM0)

bit	symbol	description	Reset value
31:9	-	Reserved	-
8:1	MASK	Mask bits 0: The bit address is not compared 1: Compare the bit address	0xFF
0	-	Reserved	-

18.5.10 I2C Software Reset Register (RST)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	RST	Writes 0x07, resulting in a software reset	0x0

19. Serial Peripheral Interface Controller (SSP/SPI)

19.1 overview

Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full-duplex mode. The devices can operate in master/slave mode, communicating with each other using a 4-wire bidirectional interface. When receiving data from a peripheral device, SPI performs a serial-to-parallel conversion, and when the data is sent to the peripheral, it performs a parallel-to-serial conversion. The SPI controller can be configured as either a master or a slave.

19.2 characteristic

- Supports master or slave mode.
- Full duplex.
- The send bit length that can be configured.
- MSB priority send/receive.
- Provides 8 16-bit transmit/receive FIFOs.

19.3 Register mapping

(SSP0 base address = 0x4380_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
WITH	0x000	R/W	SSP control registers	0x0
STATE	0x004	RO	SSP status register	0x03
THAT	0x008	R/W	SSP data registers	0x0
CLK	0x00C	R/W	SSP clock control registers	0x0
IMSC	0x010	R/W	SSP interrupt enable register	0x0
RICE	0x014	RO	SSP interrupt source status register	0x8
PUT	0x018	RO	SSP enabled Interrupt status register	0x0
ICLR	0x01C	WO	SSP interrupt clear register	0x0
CSCR	0x028	R/W	SSP software chip select signal register	0x0

19.4 Register description

19.4.1 SSP Control Register (CON)

bit	symbol	description	Reset value
31:12	-	Reserved	-
11	LBM	Loopback mode enable bit 0: Normal working mode 1: Loopback mode, serial input to serial output	0x0
10	SSPEN	SSP enable bit 0: Disable 1: Enable	0x0
9	MS	Master/slave mode select bits 0: Host mode 1: Slave mode	0x0
8	SOD	The slave output disable bit valid only in slave mode 0: The SSP can output MISO 1: SSPs cannot output MISOs	0x0
7	CPH	Clock phase control bit 0: The SSP samples data at the edge of the first clock 1: The SSP samples the data at the second clock edge	0x0
6	CPO	Clock output polarity select bit 0: SPI_CLK is low when idle 1: SPI_CLK is high when idle	0x0
5:4	FRF	Frame format 0x0: SPI - Compatible Frame Format 0x1: TISS - Compatible Frame Format 0x2: Microwire - Compatible frame format 0x3: Reserved	0x0
3:0	DSS	Select bits for data transfer length 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: 4-digit length 0x4: 5 bits length 0x5: 6 bits length 0x6: 7 bits length 0x7: 8 bits length 0x8: 9 bits length 0x9: 10-bit length 0xA: 11-bit length 0xB: 12-bit length 0xC: 13-bit length 0xD: 14-bit length 0xE: 15-bit length 0xF: 16-bit length	0x0

19.4.2 SSP Status Register (STAT)

bit	symbol	description	Reset value
31:5	-	Reserved	-
4	BSY	Busy flag bit, read-only 0: SSP idle 1: The SSP is sending/receiving data or sending FIFO non-null	0x0
3	RFF	Receives FIFO full flag bits, read-only 0: Receiving FIFO is not full 1: Receiving FIFO is full	0x0
2	RNE	Receives FIFO non-empty flag bits, read-only 0: The receive FIFO is empty 1: Receive FIFO non-null	0x0
1	TNF	Sends FIFO non-full flag bits, read-only 0: Send FIFO full 1: Send FIFO not full	1
0	TFE	Sends a FIFO null flag bit, read-only 0: Send FIFO non-empty 1: Send FIFO is empty	1

19.4.3 SSP Data Register (DAT)

bit	symbol	description	Reset value
31:16	-	Reserved	-
15:0	DATA	Write data to this register, when there is no data on the bus in the send, the data will be sent out immediately; When there is data on the bus that is being sent, the data is stored in the FIFO and sent sequentially. The minimum interval between send times is 3 SSPCLK clocks. When the data length is less than 16 bits, it needs to be right-aligned. Read this register, read the most recently received data, when the data length is less than 16 bits, need to be right-aligned.	0x0

19.4.4 SSP Clock Controller (CLK)

bit	symbol	description	Reset value
31:16	-	Reserved	-
15:8	M	SSPCLK = PCLK /((M+1)×N) N is an even number of 2-254	0x0
7:0	N		0x0

19.4.5 SSP interrupt enable register (IMSC)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3	TXIM	Sends a FIFO interrupt enable bit 0: Disables sending FIFO half-empty interrupts 1: Enables the sending OF FIFO half-empty interrupt	0x0
2	RXIM	Receives the FIFO interrupt enable bit 0: Disables receiving a HALF-full interrupt from FIFO 1: Enables receive FIFO half-full interrupts	0x0
1	RTIM	Receives the FIFO timer overflow interrupt enable bit 0: Disables receiving FIFO timer overflow interrupts 1: Enables the receive FIFO timer overflow interrupt (Overflow time: 64×SSPCLK).	0x0
0	RORIM	Receives the FIFO overflow interrupt enable bit 0: Disables receiving FIFO overflow interrupts 1: Enables receive FIFO overflow interrupts	0x0

19.4.6 SSP interrupt source status register (RIS)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3	TXRIS	This bit is set when sending FIFO is at least half-empty (non-half-empty automatic clearing)	1
2	RXRIS	Bit is set when the receive FIFO is at least half full (non-half full auto clear)	0x0
1	RTRIS	This bit is set when the receive FIFO is not empty and not read till timeout	0x0
0	RORRIS	When the receive FIFO is full and another frame of data is received, the old data is lost	0x0

19.4.7 SSP enabled Interrupt status register (MIS)

bit	symbol	description	Reset value
31:4	-	Reserved	-
3	TXMIS	This bit is set is bit when the enables the transmit FIFO in half-empty, and the transmit FIFO is at least half-empty	0x0
2	RXMIS	This bit is set is bit when the receive FIFO is half full interrupt and the receive FIFO is at least half full	0x0
1	RTMIS	When the enable receive FIFO timer overflow interrupts and the receive FIFO is not empty, the timeout is not read when the bit is not read	0x0
0	RORMIS	This bit is set is bit when the receive FIFO overflow interrupt is enabled and the receive FIFO is full and another frame of data is received	0x0

19.4.8 SSP Interrupt clear register (ICLR)

bit	symbol	description	Reset value
31:2	-	Reserved	-
1	RTIC	Write 1 to clear the RTRIS flag bit	0x0
0	RORIC	Write 1 to zero the RORRIS flag bit	0x0

19.4.9 SSP Software Chip Select Signal Register (CSCR)

bit	symbol	description	Reset value
31:5	-	Reserved	-
4	SPH	Select the signal from the machine chip 0: After each frame of data transmission is completed, the chip selection signal cannot be pulled high 1: After each frame of data transmission is completed, the chip selection signal must be pulled high	0x0
3	SWCS	Software chip select signal control bit in host mode 0: Output low 1: Output high	0x0
2	SWSEL	Select signal selection in host mode 0: The chip selection signal is automatically controlled by the SPI module 1: The chip selection signal is controlled by the SWCS bit	0x0
1:0	-	Reserved	-

20. Low Speed Analog-to-Digital Conversion (ADC0)

20.1 overview

The chip contains a 12-bit, up to 24-channel successive approximation analog-to-digital converter (ADC).

20.2 characteristic

- Analog input voltage range: AVSS (VSS) ~ AVDD (VDD).
- Maximum sampling rate: 100Ksps.
- Up to 24 single-ended analog input channels.
- The single conversion time is: 18.5×T_{ADCK}.
- Single-shot mode: Performs an A/D conversion on the specified channel.
- Continuous mode: A/D conversion is performed on all selected channels.
- Supports an external input signal to trigger an ADC conversion.
- Supports interrupt after conversion is complete.
- Built-in AD conversion result comparator.
- The conversion results for each channel are stored in the corresponding data registers.
- Channel 30 can be used to test internal analog voltage signals (including OP0/1 output, PGA0/1 output, internal 1.2V reference voltage).

20.3 Feature description

20.3.1 ADC channel description

ADC channel number	ADC channel	Description
0	AN0	ADC channel 0
1	AN1	ADC channel 1
2	AN2	ADC channel 2
…	…	…
n	ANn	ADC channel n
…	…	…
29	AN29	ADC channel 29
30	AN30	Internal analog channels

Note: AN0-A N30 any combination of channels support continuous mode conversion, with the highest priority AN0 and the lowest AN30.

AN30 channel internal analog selection:

ADCICHS<2:0>	Internal analog selection	Description
0	Bandgap(1.2V)	1.2V reference source
1	OP0_OUT (Internal Signal)	The output of OP0
2	OP1_OUT (Internal Signal)	The output of OP1
3	PGA0_OUT (internal signal)	The output of PGA0
4	PGA1_OUT (internal signal)	The output of PGA1
5	VSS	Negative reference voltage
6	AVDD(VDD)	Positive reference voltage
7	AVSS(VSS)	Negative reference voltage

20.4 Register mapping

(ADC base address = 0x4300_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
ADCCON(P1B)	0x000	R/W	ADC control register	0x0
ADCCON2(P1B)	0x004	R/W	ADC control register 2	0x0
ADCHWTG(P1B)	0x008	R/W	ADC hardware trigger control register	0x0
-	0x00C	-	Reserved	-
ADCSCAN(P1B)	0x010	R/W	ADC scan register	0x0
ADCCMP0(P1B)	0x014	R/W	ADC comparator 0 control register	0x0
-	0x018	-	Reserved	-
ADCIMSC(P1B)	0x01C	R/W	ADC interrupt enable register	0x0
ADCRIS	0x020	RO	ADC interrupt source status register	0x0
ADCMIS	0x024	RO	ADC enabled Interrupt status register	0x0
ADCICLR	0x028	WO	ADC interrupts the zero register	0x0
ADCLOCK	0x02C	R/W	ADC write enable control register	0x0
-	-	-	-	-
ADCDATA0	0x080	RO	ADC channel 0 conversion result register	0x0
ADCDATA1	0x084	RO	ADC channel 1 conversion result register	0x0
ADCDATA2	0x088	RO	ADC channel 2 conversion result register	0x0
ADCDATA3	0x08C	RO	ADC channel 3 conversion result register	0x0
ADCDATA4	0x090	RO	ADC channel 4 conversion result register	0x0
ADCDATA5	0x094	RO	ADC channel 5 conversion result register	0x0
ADCDATA6	0x098	RO	ADC channel 6 conversion result register	0x0

ADCDATA7	0x09C	RO	ADC channel 7 conversion result register	0x0
ADCDATA8	0x0A0	RO	ADC channel 8 conversion result register	0x0
ADCDATA9	0x0A4	RO	ADC channel 9 conversion result register	0x0
ADCDATA10	0x0A8	RO	ADC channel 10 conversion result register	0x0
ADCDATA11	0x0AC	RO	ADC channel 11 conversion result register	0x0
ADCDATA12	0x0B0	RO	ADC channel 12 conversion result register	0x0
ADCDATA13	0x0B4	RO	ADC channel 13 conversion result register	0x0
ADCDATA14	0x0B8	RO	ADC channel 14 conversion result register	0x0
ADCDATA15	0x0BC	RO	ADC channel 15 conversion result register	0x0
ADCDATA16	0x0C0	RO	ADC channel 16 conversion result register	0x0
ADCDATA17	0x0C4	RO	ADC channel 17 conversion result register	0x0
ADCDATA18	0x0C8	RO	ADC channel 18 conversion result register	0x0
ADCDATA19	0x0CC	RO	ADC channel 19 conversion result register	0x0
ADCDATA20	0x0D0	RO	ADC channel 20 conversion result register	0x0
ADCDATA21	0x0D4	RO	ADC channel 21 conversion result register	0x0
ADCDATA22	0x0D8	RO	ADC channel 22 conversion result register	0x0
ADCDATA23	0x0DC	RO	ADC channel 23 conversion result register	0x0
ADCDATA24	0x0E0	RO	ADC channel 24 conversion result register	0x0
ADCDATA25	0x0E4	RO	ADC channel 25 conversion result register	0x0
ADCDATA26	0x0E8	RO	ADC channel 26 conversion result register	0x0
ADCDATA27	0x0EC	RO	ADC channel 27 conversion result register	0x0
ADCDATA28	0x0F0	RO	ADC channel 28 conversion result register	0x0
ADCDATA29	0x0F4	RO	ADC channel 29 conversion result register	0x0
ADCDATA30	0x0F8	RO	ADC channel 30 conversion result register	0x0

Note:

1) The registers marked (P1B) are protected registers.

2) (P1B): When LOCK=55H, the labeled register is allowed to write; = Other values, forbidden to write.

20.5 Register description

20.5.1 ADC Control Register (ADCCON)

bit	symbol	description	Reset value
31:19	-	Reserved	-
18:16	ADCICHS	ADC internal analog selection (connected to AN30 channels). 000: Bandgap 001: OP0_OOUT 010: OP1_OUT 011: PGA0_OUT 100: PGA1_OUT 101: VSS 110: AVDD (ADC Reference Positive End VDD) 111: AVSS (ADC reference negative VSS).	0x0
15:5	-	Reserved	0x0
4	ADCEN	The ADC enable control bit 0: Disable 1: Enable	0x0
3	ADCMS	ADC mode select bit 0: Single conversion 1: Continuous conversion	0x0
2:0	ADCDIV	ADC clock prescaler selection bit $F_{ADC} = PCLK/2^{ADCDIV}$	0x0

20.5.2 ADC Control Register 2 (ADCCON2)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7	ADCST	ADC conversion starts (hardware is automatically cleared to zero after conversion) 0: The conversion is over or the ADC is in idle mode (Invalid to write 0) 1: Start the conversion (ADCEN must be 1)	0x0
6:0	-	Reserved	-

20.5.3 ADC Scan Register (ADCSCAN)

bit	symbol	description	Reset value
31	-	Reserved	0x0
30:0	ADCEn	ADC channel n enable bit (n=30-0) 0: Disable 1: Enable	0x0

20.5.4 ADC Hardware Trigger Control Register (ADCHWTG)

bit	symbol	description	Reset value
31:18	-	Reserved	-
17	ADCEXTAT	ADC external trigger enable bit 0: Disable 1: Enable	0x0
16	ADCEXTES	ADC external trigger edge selection bit 0: Drop the edge 1: Rising edge	0x0
15	ADCINTTGEN	The ADC internal function trigger enable bit 0: Disable 1: Enable	0x0
14:12	ADCINTTGSS	The internal function of the ADC triggers the source channel selection bit 000: ADC0 converts the end signal 001: ADC1 converts the end signal 010: ACMP0 event 011: ACMP1 events 100: Timer0 Interrupt Signal 101: Timer1 Interrupt Signal 11x: Reserved	0x0
11:0	-	Reserved	-

20.5.5 ADC conversion result register (ADCDATAx) x=0~30

bit	symbol	description	Reset value
31:12	-	Reserved	-
11:0	RSLT	ADC conversion results	0x0

20.5.6 ADC compares control register 0 (ADCCMPx) x=0

bit	symbol	description	Reset value
31	ADCCMPxEN	ADC comparator x enable bit 0: - 1: Enable	0x0
30	ADCCMPxO	ADC comparator x result bits (read-only) (The selected channel is automatically updated after conversion is completed). 0: The conditions for comparison are not met 1: The comparison criteria are met	0x0
29:	-	Reserved	-
28	ADCCMPxCOND	ADC comparator x compares conditional selection bits 0: ADC results < presets 1: ADC result > = preset	0x0
27:24	ADCCMPxMCNT	ADC comparator x number of matches preset When the analog-to-digital conversion result of the specified channel matches the comparison condition, the internal counter is incremented by 1, and when the internal counter is equal to the value of ADCCMPxMCNT+1, the internal counter value is automatically cleared. An ADC comparison event is generated at the same time as the match. Note:	0x0

		- ADC Comparator 0 Compare Event will place the interrupt flag ADCCMP0IF as 1;	
23:21	-	Reserved	0x0
20:16	ADCCMPxCHS	ADC comparator x compares channel selection bits 00000- Channel 0 …… …… 11110- Channel 30	0x0
15:12	-	Reserved	-
11:0	ADCCMPxDATA	ADC comparator x data preset (12 bits).	0x0

20.5.7 ADC Interrupt Enable Register (ADCIMSC)

bit	symbol	description	Reset value
31	ADCIMSC31	ADC comparator 0 interrupt enable bit 0: Disable 1: Enable	0x0
30:0	ADCIMSCn	ADC channel n interrupt enable bit (n=30-0) 0: Disable 1: Enable	0x0

20.5.8 ADC Interrupt Source Status Register (ADCRIS)

bit	symbol	description	Reset value
31	ADCRIS31	ADC comparator 0 interrupt source state 0: The interrupt source did not produce an interrupt 1: The interrupt source produces the interrupt	0x0
30:0	ADCRISn	ADC channel n interrupt source state (n=30-0) 0: The interrupt source did not produce an interrupt 1: The interrupt source produces the interrupt	0x00

20.5.9 ADC Enabled Interrupt Status Register (ADCMIS)

bit	symbol	description	Reset value
31	ADCMIS31	ADC comparator 0 interrupt state 0: No interrupt was generated 1: Enables and produces an interrupt	0x0
30:0	ADCMISn	ADC channel n interrupt state (n=30-0) 0: No interrupt was generated 1: Enables and produces an interrupt	0x0

20.5.10 ADC Interrupt clear register (ADCICLR)

bit	symbol	description	Reset value
31	ADCICLR31	Write 1 clear ADC comparator 0 interrupt state Writing 0 does not affect	0x0
30:0	ADCICLRn	Write 1 to clear the ADC channel n interrupt status Writing 0 does not affect (n=30-0)	0x0

20.5.11 ADC write enable control register (ADCLOCK)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	LOCK	When LOCK=0x55, enables the operation of the ADC-related registers (See ADC register mapping for details) When LOCK=other values, operation of ADC-related registers is prohibited	0x0

21. Fast analog-to-digital conversion (ADC1)

21.1 overview

The chip contains a 12-bit, up to 24 external channel successive approximation analog-to-digital converters (ADC1).

21.2 characteristic

- Analog input voltage range: AVSS(VSS) ~ AVDD(VDD).
- Maximum sampling rate: 1. 2Msps。
- Up to 24 single-ended analog input channels.
- The single conversion time is: 23×T_{ADCK} (sampling time is set to 10.5×T_{ADCK}).
- Single-shot mode: Performs an A/D conversion on the specified channel.
- Continuous mode: A/D conversion is performed on all selected channels.
- Supports an external input signal to trigger an ADC conversion.
- Supports interrupt after conversion is complete.
- Built-in AD conversion result comparator.
- The conversion results for each channel are stored in the corresponding data registers.
- Channel 30 can be used to test internal analog voltage signals (including OP0/1 output, PGA0/1 output, internal 1.2V reference voltage).

21.3 Feature description

21.3.1 ADC channel

ADC channel number	ADC channel	Description
0	AN0	ADC channel 0
1	AN1	ADC channel 1
2	AN2	ADC channel 2
…	…	…
n	ANn	ADC channel n
…	…	…
29	AN29	ADC channel 29
30	AN30	Internal analog channels

Note: AN0-A N30 any combination of channels support continuous mode conversion, with the highest priority AN0 and the lowest AN30.

AN30 channel internal analog selection:

ADCICHS<2:0>	Internal analog selection	Description
0	Bandgap(1.2V)	1.2V reference source
1	OP0_OUT (internal signal)	The output of OP0
2	OP1_OUT (internal signal)	The output of OP1
3	PGA0_OUT (internal signal)	The output of PGA0
4	PGA1_OUT (internal signal)	The output of PGA1
5	VSS	Negative reference voltage
6	AVDD(VDD)	Positive reference voltage
7	AVSS(VSS)	Negative reference voltage

21.3.2 ADC calibration

Before the ADC measures the analog voltage, it is recommended that the ADC module to be calibrated for higher performance and resolution. The calibration method is as follows:

1) Set the speed and sample-and-hold time of the ADC's internal comparator
2) Set the clock division of the ADC
3) Turn on the enable bit of the ADC
4) Turn on the calibration enable bit ADCCALEN for the ADC
5) After the calibration is completed, the ADCCALEN hardware is automatically cleared and the calibration process is completed

Calibration time approx.: 4096×T_{ADC} (T_{ADC} is the conversion clock of the ADC).

After calibration, initiate normal ADC conversion, keep ADCALCONV=0, and enable ADC conversion operation with calibration data

21.3.3 ADC software starts

Writing 1 in register ADCCON2.ADCST bit initiates the ADC conversion. After the conversion is complete, the bit hardware is automatically cleared to zero.

During an ADC conversion, any software and hardware triggering start signals are ignored.

21.3.4 The ADC hardware trigger start

Trigger Source:

In addition to software-initiated conversion, ADCs can also trigger ADC conversions through hardware. The types of hardware trigger sources are:

- External triggering
- Internal triggering
- EPWM output channel triggering
- EPWM count comparator 0 triggered
- EPWM count comparator 1 triggered

Different types of trigger sources can be valid at the same time, the same kind of trigger sources may contain different trigger signals, such as EPWM output channel trigger, you can choose one of the EPWM0-EPWM5 trigger signal.

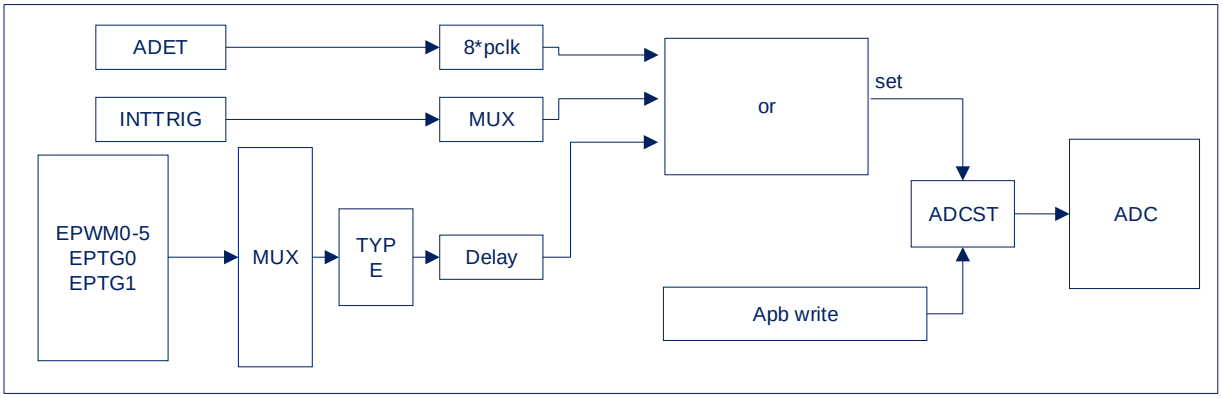


Figure 21-1: ADC hardware triggers boot

External trigger:

External trigger can choose to start the ADC on the rising or falling edge, after detecting the external trigger signal, after filtering by 2 PCLK clocks, the ADCST will be set to 1 to start the ADC conversion.

Internal trigger:

Internal triggers include: ADC0, ADC1, ACMP0, ACMP1, TIMER0/1 trigger.

ADC0: The conversion of ADC0 ends

ADC1: The conversion of ADC1 ends

ACMP0: The event output of ACMP0

ACMP1: The event output of ACMP1

Timer0: Enabled Interrupt for Timer0 (TMR0MIS)

Timer1: Enabled interrupt for Timer1 (TMR0MIS)

EPWM output channel triggering:

EPWM output channel trigger can select the rising edge, falling edge, zero, period point to start the ADC, if the EPWM trigger signal is detected, you can choose to start the ADC conversion after a certain delay. If the output channel of EPWM is remapped, the EPWM trigger signal is the signal before remapping, IPGn signal.

EPWM output channel triggering allows individual ADC conversion channels to be set. That is, after the EPWM output channel trigger signal is generated, it will be converted according to the unique configured channel. The conversion channel of the EPWM output channel that triggers the ADC is set in the ADCCHEPWM register. After the conversion is complete, it will revert to the channel settings in ADCSCAN.

EPWM counter comparator trigger:

The EPWM count comparator 0/1 trigger can be set to trigger the start-up ADC at any time during the EPWMn cycle in the same way as the EPWM channel trigger, or it can choose to start the ADC conversion after a certain delay.

The EPWM count comparator 0/1 trigger allows individual ADC conversion channels to be set. That is, after the trigger signal is generated, it will be converted according to the individual setting channel. The EPWM count comparator 0 triggers the conversion channel of the ADC set in the ADCCHEPTG0 register. The conversion channel of the EPWM count comparator 1 triggering the ADC is set in the ADCCHEPTG1 register.

After the conversion is complete, it will revert to the channel settings in ADCSCAN.

EPWM trigger delay:

The ADCEPWMTGDLY register determines when EPWM triggers the start ADC delay:

(ADCEPWMTGDLY[7:0]+2) × PCLK (Zero/EPWM Comparator 0/EPWM Comparator 1).

(ADCEPWMTGDLY [7:0]+3) × PCLK (rising/falling edge/period point).

The range of EPWM trigger delay is as follows:

PCLK	48MHz	64MHz
Delay	0.02us ~ 5.35us	0.02us ~ 4.01us

If ADCPWMTGDLY=0, the ADC conversion is initiated by delaying one PCLK clock.

EPWM triggers the initiation of the ADC configuration

EPWM-triggered ADC conversion has special time requirements in some applications. For this requirement, the ADC supports different EPWM trigger conditions within the ADC to set up independent conversion channels. For example:

EPWM output channel triggering selectable AN0, AN1, AN2 channel conversion

EPWM comparator 0 triggers selectable AN18 channel conversion

EPWM comparator 1 triggers selectable AN19 channel conversion

The channels selected for software startup or other trigger startup are AN5, AN6, AN7, AN8.

When there is no EPWM trigger condition, the default conversion channel is AN5-AN8.

If the OUTPUT channel of EPWM is triggered, only 3 channels of AN0-AN2 will be selected for AD conversion, and the CONVERSION will be automatically switched to AN5-AN8 channel enable.

If the EPWM's comparison 0 is triggered, only the AN18 channel is selected for AD conversion, and after the conversion is completed, it is automatically switched to AN5-AN8 channel enable.

If the COMPARISON 1 of EPGWM is triggered, only the AN19 channel is selected for AD conversion, and after the conversion is completed, it is automatically switched to AN5-AN8 channel enable.

It is important to note that any other trigger signals will be ignored during the period when the AD conversion is not finished.

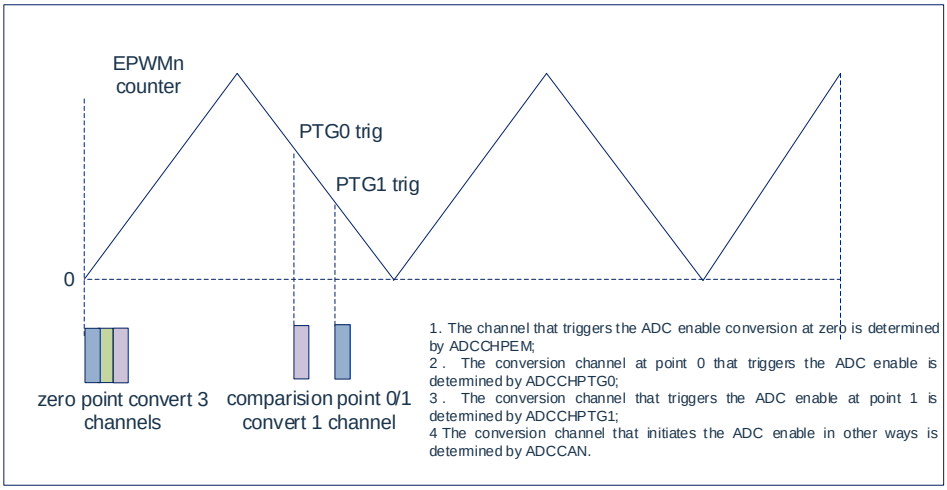


Figure 21-2: EPWM triggers the start-up ADC setup

21.4 Register mapping

(ADC1 base address = 0x4D80_0000).

RO: read-only, WO: write-only, R/W: read-write

register	Offset	R/W	description	Reset value
ADCCON(P1B)	0x000	R/W	ADC control register	0x0
ADCCON2(P1B)	0x004	R/W	ADC control register 2	0x0
ADCHWTG(P1B)	0x008	R/W	ADC hardware trigger control register	0x0
ADCPWMTGDLY(P1B)	0x00C	R/W	ADC EPWM triggers the delay data register	0x0
ADCSCAN(P1B)	0x010	R/W	ADC scan register	0x0
ADCCMP0(P1B)	0x014	R/W	ADC comparator 0 controls the register	0x0
-	0x018	R/W	Reserved	0x0
ADCIMSC(P1B)	0x01C	R/W	ADC interrupt enable register	0x0
ADCRIS	0x020	RO	ADC interrupt source status register	0x0
ADCMIS	0x024	RO	The ADC enabled Interrupt status register	0x0
ADCICLR	0x028	WO	ADC interrupt clear register	0x0
ADCLOCK	0x02C	R/W	The ADC write enable control register	0x0
ADCCHEPWM(P1B)	0x030	R/W	The ADCEPWM output trigger conversion channel registers	0x0
ADCCHPTG0(P1B)	0x034	R/W	ADC EPWM comparator 0 trigger conversion channel registers	0x0
ADCCHPTG1(P1B)	0x038	R/W	The ADC EPWM comparator trigger conversion channel register	0x0
-	-	-	-	-
ADCDATA0	0x080	RO	ADC channel 0 conversion result register	0x0
ADCDATA1	0x084	RO	ADC channel 1 conversion result register	0x0
ADCDATA2	0x088	RO	ADC channel 2 conversion result register	0x0
ADCDATA3	0x08C	RO	ADC channel 3 conversion result register	0x0
ADCDATA4	0x090	RO	ADC channel 4 conversion result register	0x0
ADCDATA5	0x094	RO	ADC channel 5 conversion result register	0x0
ADCDATA6	0x098	RO	ADC channel 6 conversion result register	0x0
ADCDATA7	0x09C	RO	ADC channel 7 conversion result register	0x0
ADCDATA8	0x0A0	RO	ADC channel 8 conversion result register	0x0
ADCDATA9	0x0A4	RO	ADC channel 9 conversion result register	0x0
ADCDATA10	0x0A8	RO	ADC channel 10 conversion result register	0x0
ADCDATA11	0x0AC	RO	ADC channel 11 conversion result register	0x0
ADCDATA12	0x0B0	RO	ADC channel 12 conversion result register	0x0
ADCDATA13	0x0B4	RO	ADC channel 13 conversion result register	0x0
ADCDATA14	0x0B8	RO	ADC channel 14 conversion result register	0x0
ADCDATA15	0x0BC	RO	ADC channel 15 conversion result register	0x0
ADCDATA16	0x0C0	RO	ADC channel 16 conversion result register	0x0
ADCDATA17	0x0C4	RO	ADC channel 17 conversion result register	0x0
ADCDATA18	0x0C8	RO	ADC channel 18 conversion result register	0x0
ADCDATA19	0x0CC	RO	ADC channel 19 conversion result register	0x0
ADCDATA20	0x0D0	RO	ADC channel 20 conversion result register	0x0
ADCDATA21	0x0D4	RO	ADC channel 21 conversion result register	0x0
ADCDATA22	0x0D8	RO	ADC channel 22 conversion result register	0x0
ADCDATA23	0x0DC	RO	ADC channel 23 conversion result register	0x0
ADCDATA24	0x0E0	RO	ADC channel 24 conversion result register	0x0
ADCDATA25	0x0E4	RO	ADC channel 25 conversion result register	0x0
ADCDATA26	0x0E8	RO	ADC channel 26 conversion result register	0x0

ADCDATA27	0x0EC	RO	ADC channel 27 conversion result register	0x0
ADCDATA28	0x0F0	RO	ADC channel 28 conversion result register	0x0
ADCDATA29	0x0F4	RO	ADC channel 29 conversion result register	0x0
ADCDATA30	0x0F8	RO	ADC channel 30 conversion result register	0x0

Note:

1) The registers marked (P1B) are protected registers.

2) (P1B): When LOCK=55H, the labeled register is allowed to write; = Other values, forbidden to write.

21.5 Register description

21.5.1 ADC Control Register (ADCCON)

bit	symbol	description	Reset value
31	ADCRST	The ADC module reset control bit 0: - 1: ADC module reset	0x0
31:26	-	Reserved	0x0
25	ADCCONVER	ADC conversion error flag bit 0: - 1: An error occurred in the ADC conversion	0x0
24	ADCCALERR	ADC calibration error flag bit 0: - 1: There was an error in the ADC calibration	0x0
23:22	-	Reserved	0x0
21	ADCCONVERRCLR	The ADC conversion error flag is clear bit 0: - 1: Clear the ADCCONVERR bit	0x0
20	ADCCALERRCLR	The ADC calibration error flag clear bit 0: - 1: Clear the ADCCONVERR bit	0x0
19	-	Reserved	-
18:16	ADCICHS	ADC internal analog selection (connected to AN30 channels). 000: Bandgap 001: OP0_OOUT 010: OP1_OUT 011: PGA0_OUT 100: PGA1_OUT 101: VSS 110: AVDD (ADC Reference Positive End VDD) 111: AVSS (ADC reference negative VSS).	0x0
15	-	Reserved	-
14	ADCSS	ADC internal comparator speed select bit 0: FADC up to 32MHzis supported 1: Supports FADC up to 4MHz	0x0
13:12	ADCSHT	ADC sample-and-hold time selection bit 00: 3.5 ADC clock cycles 01: 4.5 ADC clock cycles 10: 6.5 ADC clock cycles 11: 10.5 ADC clock cycles	0x0
11:5	-	Must be 0	-
4	ADCEN	The ADC enable control bit 0: Disable 1: Enableion	0x0
3	ADCMS	ADC mode select bit 0: Single conversion 1: Continuous conversion (Converts all enabled ADC channels at once)	0x0
2:0	ADCDIV	ADC clock prescaler selection bit $F_{ADC} = PCLK/2^{ADCDIV}$	0x0

21.5.2 ADC Control Register 2 (ADCCON2)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7	ADCST	ADC conversion starts (hardware is automatically cleared to zero out after conversion) 0: The conversion is over or the ADC is in idle mode (Invalid to write 0) 1: Start the conversion (ADCEN must be 1)	0x0
6:2	-	Reserved	0x0
1	ADCCALCONV	ADC calibration function enables bit 0: Enables ADC conversion with calibration data 1: Disable	0x0
0	ADCCALEN	ADC calibration enable bit 0: - (Invalid to write 0) 1: Enable (auto zero after calibration is complete)	0x0

The calibration time is approximately 4096×T_{ADC} (T_{ADC} is the conversion clock of the ADC).

21.5.3 ADC Hardware Trigger Control Register (ADCHWTG)

bit	symbol	description	Reset value
31:18	-	Reserved	-
17	ADCEXTEN	ADC external trigger enable bit 0: Disable 1: Enable	0x0
16	ADCEXTES	ADC external trigger edge selection bit 0: Drop the edge 1: Rising edge	0x0
15	ADCINTTGEN	The ADC internal function trigger enable bit 0: Disable 1: Enable	0x0
14:12	ADCINTTGSS	The internal function of the ADC trigger source channel selection bit 000: ADC0 converts the end signal 001: ADC1 converts the end signal 010: ACMP0 event 011: ACMP1 events 100: Timer0 Interrupt Signal 101: Timer1 Interrupt Signal 11x: Reserved	0x0
11:10	-	Reserved	-
9	ADCPTG1EN	ADC EPWM Count Comparator 1 trigger enable bit 0: Disable 1: Enable	0x0
8	ADCPTG0EN	ADC EPWM count comparator 0 trigger enable bit 0: Disable 1: Enable	0x0
7	ADCEPWMTEN	ADC EPWM output trigger enable bit 0: Disable 1: Enable	0x0
6:4	ADCEPWMTSS	The ADC EPWM output trigger source channel selection bit	0x0

		000: The trigger source is EPWM0 001: The trigger source is EPWM1 010: The trigger source is EPWM2 011: The trigger source is EPWM3 100: The trigger source is EPWM4 101: The trigger source is EPWM5 11x: Reserved	
3:2	-	Reserved	-
1:0	ADCPEWMTPS	ADC EPWMn trigger mode selection bit (n=0-5) 00: The rising edge of the EPWMn waveform 01: EPWMn Period point (IPGn) 10: The falling edge of the EPWMn waveform 11: Zero point of EPWMn (IPGn)	0x0

21.5.4 ADC EPWM Trigger Delay Register (ADCEPWMTGDLY)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	ADCEPWMTGDLY	ADC EPWM triggers delay data EPWM trigger delay (including output channel triggering with EPWM comparator 0/1) (ADCPWMTGDLY+2) initiates ADC conversion after × PCLK (ADCST is set to 1) (ADCEPWMTGDLY=0, delay is 1×PCLK)	0x0

21.5.5 ADC Scan Register (ADCSCAN)

bit	symbol	description	Reset value
31	-	Reserved	0x0
30:0	ADCEn	ADC channel n enable bit (n=30-0) 0: Disable 1: Enable	0x0

21.5.6 ADC EPWM Output Trigger Conversion Channel Enable Register (ADCCHEPWM)

bit	symbol	description	Reset value
31	-	Reserved	-
30:0	ADCCHEPWMn	ADC EPWM output triggers conversion channel enable bit (n=30-0) 0: Disable 1: Enable	0x0

21.5.7 ADC EPWM Comparator 0 Trigger Conversion Channel Enable Register (ADCCHPTG0)

bit	symbol	description	Reset value
31	-	Reserved	-
30:0	ADCCHPTG0n	ADC EPWM comparator 0 trigger conversion channel enable bit (n=30-0) 0: Disable 1: Enable	0x0

21.5.8 ADC EPWM Comparator 1 Trigger Conversion Channel Enable Register (ADCCHPTG1)

bit	symbol	description	Reset value
31	-	Reserved	-
30:0	ADCCHPTG1n	ADC EPWM Comparator 1 Trigger Conversion Channel Enable Bit (n=30-0) 0: Disable 1: Enable	0x0

21.5.9 ADC conversion result register (ADCDATAx) x=0~30

bit	symbol	description	Reset value
31:12	-	Reserved	-
11:0	RSLT	ADC conversion result	0x0

21.5.10 ADC Comparison Control Register 0 (ADCCMP0)

bit	symbol	description	Reset value
31	ADCCMP0EN	ADC comparator 0 enable bit 0: -- 1: Enable	0x0
30	ADCCMP0O	ADC Comparator 0 Result Bits (Read Only) (The selected channel is automatically updated after the conversion is complete) 0: The conditions for comparison are not met 1: The comparison criteria are met	0x0
29	-	Reserved	0x0
28	ADCCMP0COND	ADC Comparator 0 compares conditional selection bits 0: ADC results < presets 1: ADC result > = preset	0x0
27:24	ADCCMP0MCNT	ADC comparator 0 match count preset When the analog-to-digital conversion result of the specified channel matches the comparison condition, the internal counter is incremented by 1, and when the internal counter is equal to the value of ADCCMP0MCNT+1, the internal counter value is automatically cleared. Matching generates an ADC comparison event that can be used as a signal to trigger the brake action of the EPWM. Note: ADC Comparator 0 compares events to set the interrupt flag ADCCMP0IF to 1;	0x0
23:21	-	Reserved	-
20:16	ADCCMP0CHS	ADC comparator 0 compares channel selection bits 00000: Channel 0 …… …… 11110: Channel 30	0x0
15:12	-	Reserved	0x0
11:0	ADCCMP0DATA	ADC Comparator 0 Data Preset (12 bits)	0x0

21.5.11 ADC Interrupt Enable Register (ADCIMSC)

bit	symbol	description	Reset value
31	ADCIMSC31	ADC comparator 0 interrupt enable bit 0: Disable 1: Enable	0x0
30:0	ADCIMSCn	ADC channel n interrupt enable bit (n=30-0) 0: Disable 1: Enable	0x0

21.5.12 ADC Interrupt Source Status Register (ADCRIS)

bit	symbol	description	Reset value
31	ADCRIS31	ADC comparator 0 interrupt source state 0: The interrupt source did not produce an interrupt 1: The interrupt source produces the interrupt	0x0
30:0	ADCRISn	ADC channel n interrupt source state (n=30-0) 0: The interrupt source did not produce an interrupt 1: The interrupt source produces the interrupt	0x0

21.5.13 ADC Enabled Interrupt Status Register (ADCMIS)

bit	symbol	description	Reset value
31	ADCMIS31	ADC comparator 0 interrupt state 0: No interrupt was generated 1: Enables and produces an interrupt	0x0
30:0	ADCMISn	ADC channel n interrupt state (n=30-0) 0: No interrupt was generated 1: Enables and produces an interrupt	0x0

21.5.14 ADC Interrupt Clear Register (ADCICLR)

bit	symbol	description	Reset value
31	ADCICLR31	Write 1 clear ADC comparator 0 interrupt state Writing 0 does not affect	0x0
30:0	ADCICLRn	Write 1 to zero out the ADC channel n interrupt status Writing 0 does not affect (n=30-0)	0x0

21.5.15 The ADC write enable control register (ADCLOCK)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	LOCK	When LOCK=0x55, enables the operation of the ADC-related registers (See ADC register mapping for details) When LOCK=other values, operation of ADC-related registers is prohibited	0x0

22. Operational amplifier (OP0/1, PGA0/1).

22.1 overview

The chip contains two basic op amp blocks and two programmable gain amplifiers. A small number of peripheral components can be used to achieve basic signal amplification and signal calculation functions.

22.2 characteristic

OP (Operational Amplifier)

- Each op amp is multiplexed on all three ends with the GPIO port.
- Configurable to comparator mode.
- The op amp output can be internally connected to ADC channel 30 for measurement.

PGA (Programmable Gain Amplifier).

- Adjustable gain: 4X/8X/10X/12X/14X/16X/32X.
- The PGA output can be internally connected to ADC channel 30 for measurement.

22.3 Function description

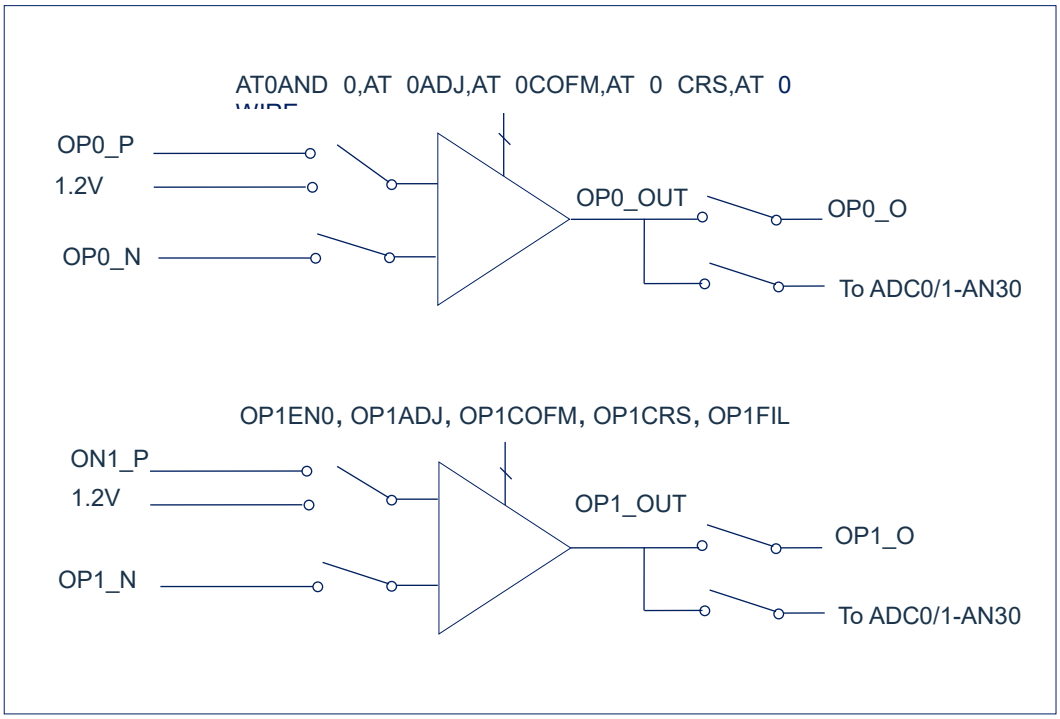


Figure 22-1: Op Amp vs. PGA Structure Diagram (1).

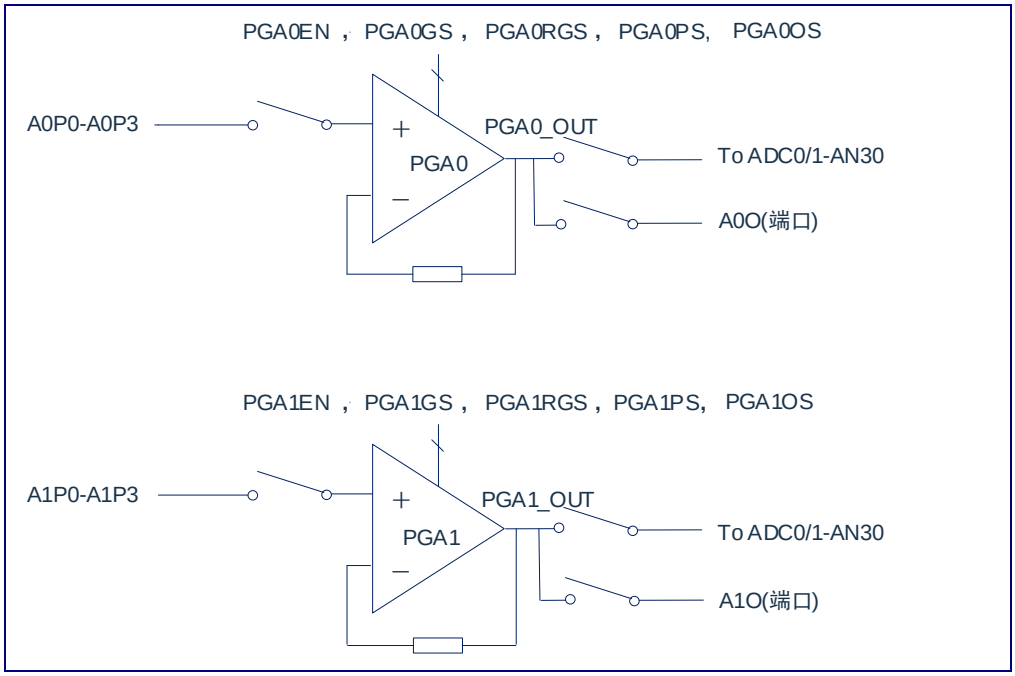


Figure 22-2 Op Amp and PGA Structure Diagram (2).

22.4 Register mapping

(OP0 base address = 0x4C80_0000; OP1 base address = 0x4C80_000C).

RO: read-only, WO: write-only, R/W: read-write

register	Offset	R/W	description	Reset value
WITH0	0x000	R/W	OP control register 0	0x0
CON1	0x004	R/W	OP control register 1	0x10
ADJE	0x008	R/W	OP regulate control register	0x0

(PGA0 base address = 0x4C80_0018; PGA1 base address = 0x4C80_0024).

RO: read-only, WO: write-only, R/W: read-write

register	Offset	R/W	description	Reset value
WITH	0x000	R/W	PGA control registers	0x0

22.5 Register description

22.5.1 Op amp n control register 0 (CON0) (n=0-1)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7	OPnEN	Op amp n enable bit 0: Disable 1: Enable	0x0
6	OPnCOFM	Op amp n mode enable bit 0: Disable 1: Enable	0x0
5	OPnFIL	Op amp n operating mode selection 0: Op amp mode (OPnCOFM must be 0). 1: Comparison mode (OPnCOFM must be 0).	0x0
4	ThePnOS	Op amp n output channel enable bit 0: Disable 1: OPn_O output enablement	0x0
3:2	ONanNS	Op amp n negative channel selection bit 00: ThePn_N Other: Disable	0x0
1:0	ONnPS	Op amp n positive channel selection bit 00: ThePn_P 01: 1.2V(Bandgap) Other: Disable	0x0

22.5.2 Op amp n control register 1 (CON1) (n=0-1)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7	OPnOUT	Op amp n adjusts the resulting bit/comparator mode output (read-only)	0x0
6	OPnCRS	Op amp n mode input select bit 0: Negative-side input 1: Positive input	0x0
5	-	Reserved	-
4:0	ONanADJ	Op amp n offset voltage select bit	0x10

22.5.3 The op amp n adjust enable control register (ADJE) (n=0-1)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	ONnADJE	Op amp n offset adjustment enable bit AA: This is determined by the OPnADJ < 4:0 > in the OPnCON1 register Other: Determined by the CONFIG relevant bit	0x0

22.5.4 PGAn Control Register (CON) (n=0-1)

bit	symbol	description	Reset value
31:16	-	Reserved	-
15	PGAnEN	PGAn enable bit 0: Disable 1: Enable (PGA0EN must also be 1 if only PGA1 is used).	0x0
14:12	PGAnGS	PGAn gain select bit 000: 4x 001: 8x 010: 10x 011: 12x 100: 14x 101: 16x 11x: 32x	0x0
11	PGAnRGS	PGAn feedback resistor ground selection 0: The ground connected to the module 1: Connect to the dedicated ground wire PIN	0x0
10	-	Reserved	-
9:8	PGAnOS	PGAn output channel enable bit 00: Disable 01: AnO output enabled Other: forbidden	0x0
7:4	PGAnPS	PGAn positive channel selection bit 00: AnP0 01: AnP1 10: AnP2 11: AnP3	0x0
3:0	-	Reserved	-

23. Analog comparator (ACMP0/1)

23.1 overview

Inside the chip are two analog comparators. The comparator can be configured for different applications. When the positive voltage is greater than the negative voltage, the comparator outputs logic 1 and vice versa output 0, which can also be changed by the output polarity select bit. When the comparator output value changes, each comparator can be configured to generate an interrupt.

23.2 characteristic

- Analog input voltage range: 0 ~ (VDD-1.5V).
- Hysteresis voltage selection (10mV/20mV/60mV-typ) is supported.
- Each comparator positive terminal can select 4 port inputs.
- Each comparator negative terminal can select the port input and internal reference voltage.
- The internal reference voltage VREF selects the divider output of the internal Bandgap (1.2V) and VDD.
- Internal reference voltage divider range: (2/20) ×VREF~ (17/20) ×VREF with a total of 16 gears.
- Output filterable time can be selected: 0 ~ 512× Tsys.
- Output changes can produce interrupts.

23.3 Function description

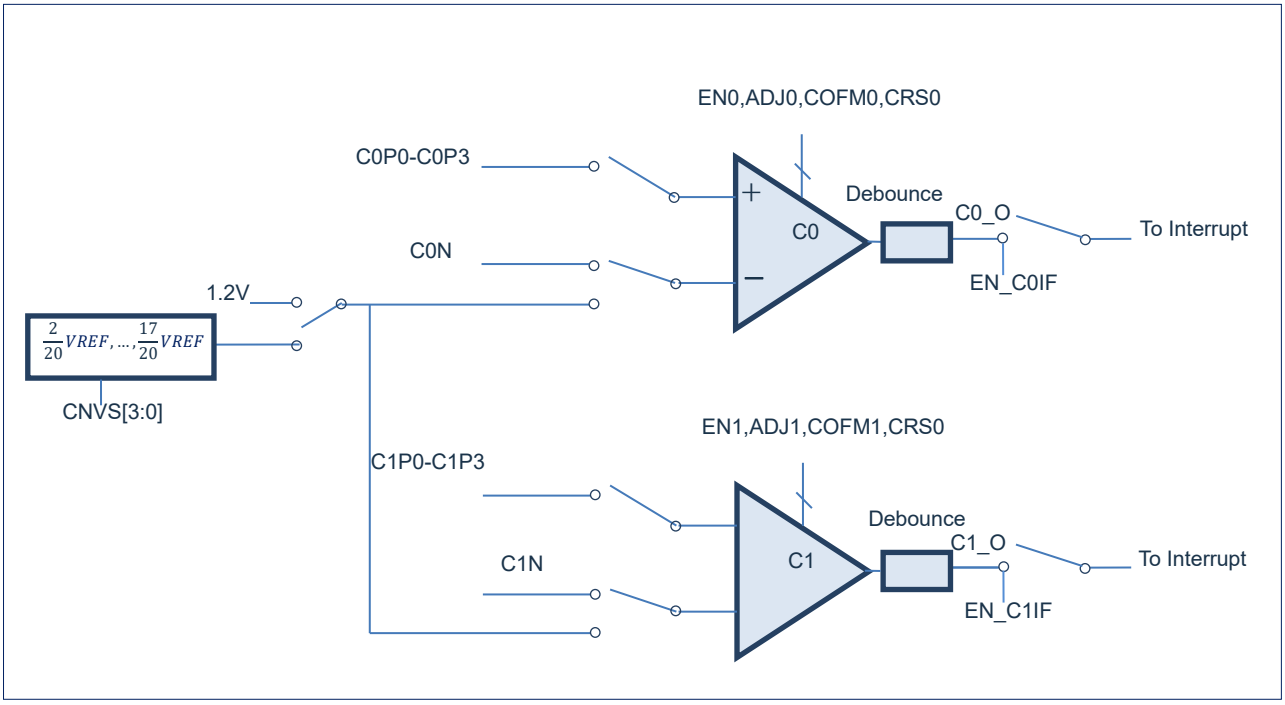


Figure 23-1: Comparator Block Diagram

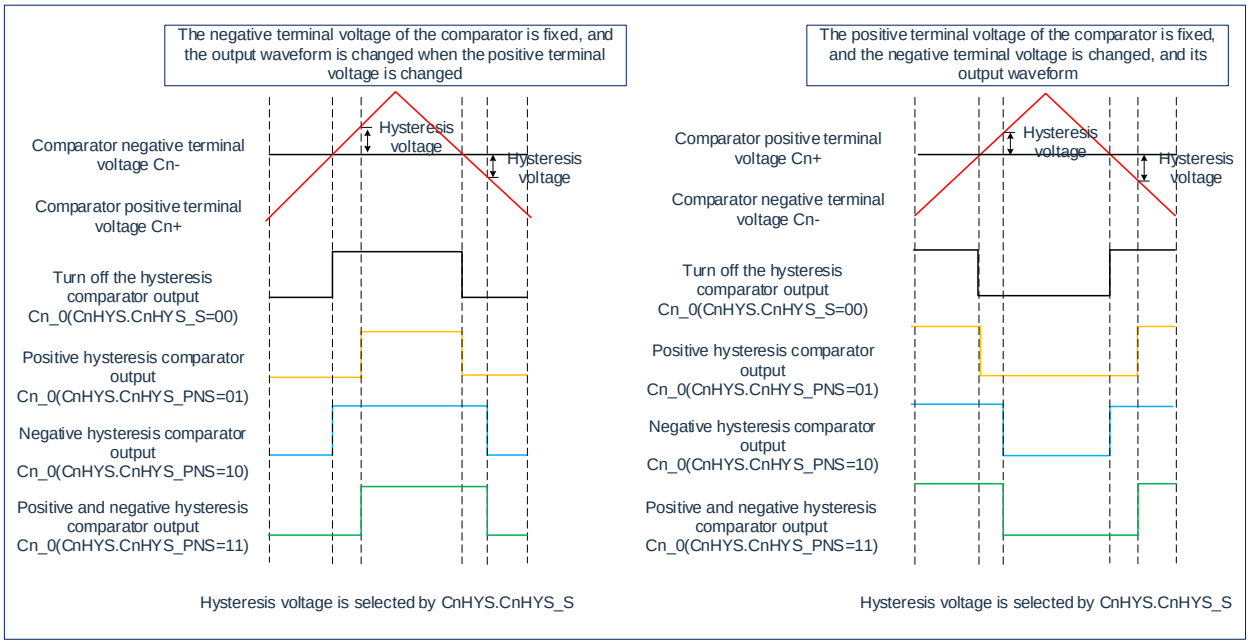


Figure 23-2: Block diagram of the comparator hysteresis function

23.4 Register mapping

(ACMP base address = 0x4D00_0000). RO: read-only, WO: write-only, R/W: read-write

register	Offset	R/W	description	Reset value
C0CON0(P1B)	0x000	R/W	Analog comparator 0 control register 0	0x0
C0CON1(P1B)	0x004	R/W	Analog comparator 0 control register 1	0x10
C0CON2(P1B)	0x008	R/W	Analog comparator 0 control register 2	0x0
C0ADJE(P1B)	0x00C	R/W	Analog comparator 0 adjust enable register	0x0
C1CON0(P1B)	0x010	R/W	Analog comparator 1 control register 0	0x0
C1CON1(P1B)	0x014	R/W	Analog comparator 1 control register 1	0x10
C1CON2(P1B)	0x018	R/W	Analog comparator 1 control register 2	0x0
C1ADJE(P1B)	0x01C	R/W	Analog comparator 1 adjust enable register	0x0
CVRCON(P1B)	0x020	R/W	Analog comparator reference voltage control register	0x0
CVECON(P1B)	0x024	R/W	Analog comparator event control register	0x0
IMSC(P1B)	0x028	R/W	Analog comparator interrupt enable register	0x0
RICE	0x02C	RO	The analog comparator interrupt source status register	0x0
PUT	0x030	RO	The analog comparator enabled Interrupt status register	0x0
ICLR	0x034	WO	Analog comparator interrupt clear register	0x0
LOCK	0x038	R/W	Analog comparator write enable register	0x0

Note:

1) The registers marked (P1B) are protected registers.

2) (P1B): When LOCK=55H, the labeled register is allowed to write; = Other values, forbidden to write.

23.5 Register description

23.5.1 Analog comparator n control register 0 (CnCON0) (n=0-1)

bit	symbol	description	Reset value
31:16	-	Reserved	-
15	Cnen	Analog comparator n enable bit 0: Disable 1: Enable	0x0
14	CnCOFM	Analog comparator n adjustment mode enable bit 0: Disable 1: Enable	0x0
13	CnN2GND	Analog comparator n adjustment mode negative ground enable bit 0: Disable 1: Enable	0x0
12:8	-	Reserved	-
7:4	CnPS	Analog comparator n positive channel selection bit 000: CnP0 001: CnP1 010: CnP2 011: CnP3 1xx: Prohibit selection	0x0
3:0	CnNS	Analog comparator n negative channel selection bit 00: CnN 01: Vref (Bandgap or k×VDD) 1x: forbidden	0x0

23.5.2 Analog comparator n control register 1 (CnCON1) (n=0-1)

bit	symbol	description	Reset value
31:10	-	Reserved	-
9	CnOUT	Analog comparator n result bits (Read-only).	0x0
8	CnCRS	Analog comparator n adjust mode input select bit 0: Negative side 1: Positive end	0x0
7:5	-	Reserved	-
4:0	CnADJ	Analog comparator n adjustment bit	0x10

23.5.3 Analog comparator n control register 2 (CnCON2) (n=0-1)

bit	symbol	description	Reset value
31:13	-	Reserved	-
12	CnHYSLS	Analog comparator n hysteresis mode control bit (single-ended hysteresis function is supported only). 0: Positive hysteresis 1: Negative hysteresis See the corresponding block diagram in the function description	0x0
11:10	CnHYSVS	Analog comparator n hysteresis voltage selection (invalid in regulation mode). 00: No lag 01: 10mV 10: 20mV 11: 60mV	0x0
9	CnPOS	Analog comparator n output polarity select bit 0: Normal output 1: Inverting output	0x0
8	CnFE	Analog comparator n output filtering enable bit 0: Disable 1: Enable	0x0
7:4	-	Reserved	-
3:0	CnFS	Analog comparator n output filtering time selection bit 0000: (0~1)×Tpclk 0001: (1~2)×Tpclk 0010: (2~3)×Tpclk 0011: (4~5)×Tpclk 0100: (8~9)×Tpclk 0101: (16~17)×Tpclk 0110: (32~33)×Tpclk 0111: (64~65)×Tpclk 1000: (128~129)×Tpclk 1001: (256~257)×Tpclk 1010: (512~513)×Tpclk Other: (0~1)×Tpclk	0x0

23.5.4 Analog comparator n adjust enable register (CnADJE) (n=0-1)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	CnADJE	AAH: This is determined by the OPnADJ < 4:0 > in the CnCON1 register Other: Determined by the CONFIG relevant bit	0x0

23.5.5 Analog comparator reference voltage control register (CVRCON)

bit	symbol	description	Reset value
31:6	-	Reserved	-
5:4	CSVR	Analog comparator negative reference voltage selection bit 0x: Choice 1.2V (Bandgap) 10: Select k× VDD 11: Select k×1.2V(0.12V~1.02V)	0x0
3:0	CVS	Analog comparator reference voltage divider k select bit 0000: 2/20 0001: 3/20 …… …… 1111: 17/20 Note: - The Step for the VDD divider was VDD (1/20). - Choose a Step with a 1.2V divider for 60mV	0x0

23.5.6 Analog Comparator Event Control Register (CEVCON)

bit	symbol	description	Reset value
31:6	-	Reserved	-
5	EVE1	Analog comparator 1 event output enable bit (does not affect interrupt generation) 0: Disable 1: Enable	0x00
4	EVE0	Analog comparator 0 event output enable bit (does not affect interrupt generation). 0: Disable 1: Enable	0x0
3:2	EVS1	Analog Comparator 1 events generate conditional selection bits 00: Comparator 1 outputs a jump from 0->1 01: Comparator 1 outputs a jump from 1->0 10: Comparator 1 outputs a jump from 0->1 or a transition from 1->0 11: Reserved	0x0
1:0	EVS0	Analog comparator 0 events produce conditional selection bits 00: Comparator 0 outputs a jump from 0->1 01: Comparator 0 outputs a jump from 1->0 10: Comparator 0 outputs a jump from 0->1 or a transition from 1->0 11: Reserved	0x0

23.5.7 Analog comparator interrupt enable register (IMSC)

bit	symbol	description	Reset value
31:2	-	Reserved	-
1	EN_C1IF	Analog comparator 1 interrupt enable bit 0: Disable 1: Enable	0x0
0	EN_C0IF	Analog comparator 0 interrupt enable bit 0: Disable 1: Enable	0x0

23.5.8 Analog comparator interrupt source status register (RIS)

bit	symbol	description	Reset value
31:2	-	Reserved	-
1	RIS_C1IF	Analog Comparator 1 interrupt source state bit 0: No interrupt was generated 1: An interrupt has been generated (event generation).	0x0
0	RIS_C0IF	Analog comparator 0 interrupt source status bit 0: No interrupt was generated 1: An interrupt has been generated (event generation).	0x0

23.5.9 Analog comparator enabled interrupt source status register (MIS)

bit	symbol	description	Reset value
31:2	-	Reserved	-
1	MIS_C1IF	Analog Comparator 1 enabled Interrupt state bit 0: No interrupt was generated 1: An interrupt has been generated	0x0
0	MIS_C0IF	Analog comparator 0 enabled Interrupt state bit 0: No interrupt was generated 1: An interrupt has been generated	0x0

23.5.10 Analog comparator interrupt clear control register (ICLR)

bit	symbol	description	Reset value
31:2	-	Reserved	-
1	ICLR_C1IF	Analog comparator 1 interrupt clear control bit Write 0: Does not affect Write 1: Clear the RIS_ the C1IF flag bit	0x0
0	ICLR_C0IF	Analog comparator 0 interrupt clear control bit Write 0: Does not affect Write 1: Clear the RIS_ the C0IF flag bit	0

23.5.11 Analog comparator write enable control register (LOCK)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	LOCK	When LOCK=0x55, enables the operation of acMP-related registers (See ACMP register mapping instructions for details). When LOCK=other values, operation of ACMP-related registers is prohibited	0

24. Memory Control Module (FMC)

24.1 overview

On-chip FLASH with a maximum of 32KB for storing applications. A user configuration area for system initialization. Supports the need for external reset when switching between the bootloader and the user program after application programming (IAP), updating the FLASH program.

24.2 characteristic

- Supports up to 32KB of application storage space (APROM).
- Support BOOT function, BOOT area and APROM share a maximum of 32KB of space, the size can be set to 1KB/2KB/4KB.
- Supports a 1KB data storage area and does not take up program space.
- Supports 512-byte page erase for all on-chip FLASH operations.
- Supports On-Chip Programming (ISP)/In-Application Programming (IAP) to update on-chip FLASH.
- Supports CRC checksum calculation and detection of program space codes of any interval.

24.3 Feature description

24.3.1 Memory structure

The On-Chip FLASH Contains the maximum 32KB User program area (APROM），512 Byte User Configuration Area (User Configuration).

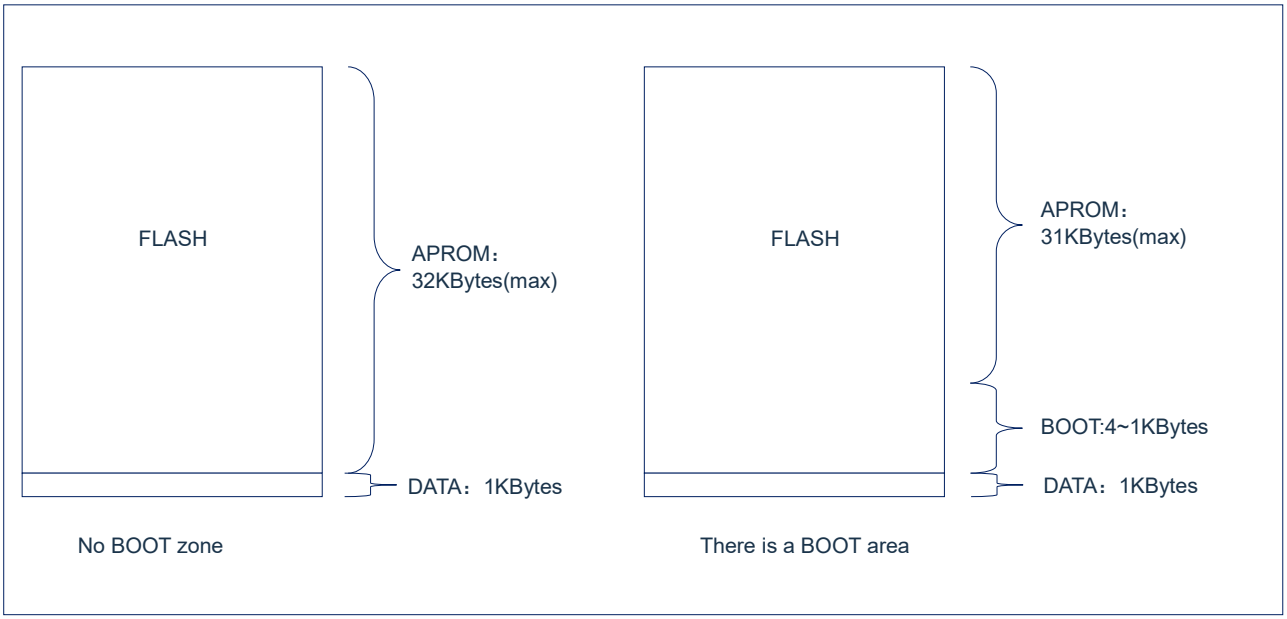


Figure 24-1: Storage structure diagram

24.3.2 Flash's operation

Erase: Includes two commands: overall erase and page erase.

1) When erased as a whole, the entire APROM space is erased. The overall erase operation method is as follows:
   - Enables access to FMC-related registers.
   - Wait for the FMC to idle.
   - Writes 0x06 in FMCCMD.
   - Wait for the FMC to idle.
   - Disable access to FMC-related registers.

2) When a page is erased, each page can erase 0x200 address space. Here's how to do page erasure:
   - Enables access to FMC-related registers.
   - Write the page erase header address in FMCADR.
   - Wait for the FMC to idle.
   - Writes 0x03 in FMCCMD.
   - Wait for the FMC to idle.
   - Disable access to FMC-related registers.

Programming: After the erase is complete, the page data can be programmed continuously. The programming is as follows:

1) Enables access to FMC-related registers.
2) Set the address that needs to be programmed in FMCADR.
3) Write the data that needs to be programmed in FMCDAT.
4) Wait for the FMC to idle.
5) Writes 0x02 in FMCCMD.
6) Wait for the FMC to idle.
7) Disable access to FMC-related registers.

Read: Contains two ways to read:

1) Direct addressing, which directly reads the 0x0000-0x7FFF address.
2) Read by FMC command, the operation sequence is as follows:
   - Enables access to FMC-related registers.
   - Set the address to be read in FMCADR.
   - Writes 0x01 in FMCCMD.
   - Read the FMCDAT value.
   - Disable access to FMC-related registers.

24.3.3 Flash space CRC check

See < security-related > sections for details.

24.3.4 Flash space program startup selection

The chip can be configured to boot from APROM or from the BOOT zone after power-on reset. The relevant selections are selected in the user configuration area:

BOOT_TYPE	Power-on boot selection Description
1111	Boot from APROM
0001	Boot from theBOOT area
0000	Booting from theBOOT region requires theBOOT pin to be grounded
other	Boot from APROM

If you need to boot from BOOT, you need to allocate a valid space to the BOOT area: 1KBytes/2KBytes/4Kbytes.

If the space allocated by BOOT is 0 KBytes, even if BOOT_TYPE chooses to start from the BOOT area, it is actually started from APROM.

After choosing to start from the BOOT area to complete the bootloader, if you need to go to APROM program execution, it is recommended to perform the following steps:

1) Write the ISPS bit of the FMCCON register to 1, allowing the next reset procedure to be executed from APROM.
2) Write the RSTCON register to 0x55AA669A, allowing the system to reset (without reloading the boot configuration).
3) After the system resets, the program will be executed from the APROM area.

After the program is run in APROM, if it is necessary to go to the BOOT area for execution, it is recommended to perform the following steps:

1) Write the ISPS bit of the FMCCON register to 0, allowing the next reset procedure to be executed from the BOOT area.
2) Write the RSTCON register to 0x55AA669A, allowing the system to reset (without reloading the boot configuration).
3) After the system resets, the program will be executed from the BOOT area.

24.4 Register mapping

(FMC base address = 0x4980_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
CON(P1D)	0x000	R/W	FMC control register	-
ADR(P1D)	0x004	R/W	FMC address register (FMC CRC checks the start address register).	0x0
DAT(P1D)	0x008	R/W	FMC data register	0x0
CMD(P1D)	0x00C	R/W	FMC command register	0x0
LOCK	0x010	R/W	FMC accesse enable register	0x0
CRCEA(P1D)	0x020	R/W	FMC CRC checksum end address register	0xFFFF
CRCIN(P1D)	0x024	R/W	FMC CRC input register	0x0
CRCD(P1D)	0x028	R/W	FMC CRC data register	0x0

Note:

1) The registers marked (P1D) are protected registers.
2) (P1D): When LOCK=55AA6699H, the marked register is allowed to write; = Other values, forbidden to write.

24.5 Register description

24.5.1 FMC Control Register (CON)

bit	symbol	description	Reset value
31:6	-	Reserved	-
5	BUSY	FMC busy flag bit 0: FMC idle 1: The FMC is busy and performs erase, programming, or reading operations normally	0x0
4	ISPS	Select the location where the program starts after the next reset (Excluding power-on reset, MCURST reset, external reset). 0: After reset, the program is executed from BOOT (BOOT region and BOOT enable need to be configured). 1: After the reset the procedure is performed from the APROM	1
3:0	-	Reserved	-

24.5.2 FMC Address Register (ADR)

bit	symbol	description	Reset value
31:0	ADDR	The word operation address (or the starting address of the CRC check operation). 0x00xx_xxxx（is APROM） 0x1cxx_xxxx (is DATA region) (The lower two digits must be 00).	0x0

24.5.3 FMC Data Register (DAT)

bit	symbol	description	Reset value
31:0	FMCDAT	When a write operation is performed, the data is written to FLASH, and when a read operation is performed, the FLASH data is returned	0x0

24.5.4 FMC Command Register (CMD)

bit	symbol	description	Reset value
31:5	-	Reserved	-
4:0	FMCFUNC	FMC features 0x0: Reserved 0x1: Read the data 0x2: Write data (50us). 0x3: Page erase (4.7ms). 0xD: CRC check（CRC16-CCITT） Other: Reserved	0x0

24.5.5 FMC access enable register (LOCK)

bit	symbol	description	Reset value
31:0	FMCLOCK	Writes 0x55AA6699 enables accessing the other FMC registers; read value is 1 Write any other value, disable the operation of other FMC registers, and read value is 0	0x0

24.5.6 FMC CRC Checksum End Address Register (CRCEA)

bit	symbol	description	Reset value
31:16	-	Reserved	-
15:0	CRCEA	The CRC checksum end address	0x0

24.5.7 FMC CRC Input Register (CRCIN)

bit	symbol	description	Reset value
31:8	-	Reserved	-
7:0	CRCIN	The CRC input requires 8 bits of data to be calculated	0x0

24.5.8 FMC CRC Data Register (CRCD)

bit	symbol	description	Reset value
31:16	-	Reserved	-
15:0	CRCD	The CRC holds the 16-bit result of the operation	0x0

25. Security-related

25.1 overview

The chip supports functions related to code security and application security.

25.2 Unique Chip Identification Number (UID)

Each chip has a different 96-bit unique identification number, or Unique identification. It has been set at the factory and cannot be modified by the user. The chip UID is read through the memory module when used. (This function requires the support of the relevant departments of CMS).

There are two ways to read UIDs:

1) Read by the FMC module, the corresponding address mapping is as follows:

(Memory base address = 0x1800_0000) RO: read-only; WO: Write only; R/W: Read and write.

address	Offset	R/W	description	Reset value
Reserved	0x000	-	Reserved	-
UID0	0x004	RO	UID[31:0]	-
UID1	0x008	RO	UID[63:32]	-
UID2	0x00C	RO	UID[95:64]	-

2) Read by the system control module SYSCON, the corresponding address mapping is as follows:

(Register base address = 0x5000_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
Reserved	0x000	-	Reserved	-
CIDL	0x034	RO	UID[63:32]	-
YES	0x038	RO	UID[95:64]	-
UIDX	0x500	RO	UID[31:0]	-

25.3 User Unique Chip Identification Number (USRUID).

The chip has another 128-bit chip identification number USRUID. Includes a 96-bit user-programmable identification number and a 32-bit fixed identification number, which is distinguished from the UID by the fact that it is not readable in the USRUID program. The user can set the unique 96-digit identification number in the CMS tool. Of which the other 32bit is not operational.

The 128-bit USRUID can be used as a key in an encryption application, the user program can detect the key to establish a protection mechanism.

Mechanism to prevent decryption operation in the program: If the detection result is incorrect, the USRUID detection is immediately disabled, the re-detection operation will be ignored, only after reset detection can be activated again, and the single detection tolerance rate is 0.

USRUID has a separate encryption bit in the User Configuration area, and after setting the USRUID to the encryption state, no other method or tool can read out the data in it.

The specific methods of detection are as follows:

There are 4 registers in the system control module, namely UUIDWC0, UUIDWC1, UUIDWC2, UUIDWCS, which are used to detect USRUID data if written to UUIDWC0-UUIDWC2 (write 96bit user identification number), UUIDWCS (must write 0xFFFFFFFFF) All data is the same as the data of the preset USRUID, the values of these registers are read as 0x1, otherwise it is 0.

Mechanism to prevent decryption operation in the program: If the data written is incorrect, the USRUID detection operation is immediately disabled, and the operation of writing to the USRUID again will be ignored, and it needs to be reset to detect again, and the single detection tolerance rate is 0.

25.4 Protection of program code

The chip supports the protection function of the chip code and the code partition protection function.

APROM partition protection: The 32KBytes space is divided into 16 segments, each with a size of 2KBytes, and the protection state can be set separately in the user configuration register CFG_APROMPE. If a BOOT interval has been assigned, the protection state acts within the valid area.

APROM protection status description												
bit	address	Valid status	Read			programming			Erase			Default value
			NM	SW	BT	NM	SW	BT	NM	SW	BT	-
0	0x0000-0x07FF	0	✓	×	✓	×	×	✓	×	×	✓	1
1	0x0800-0x0FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
2	0x1000-0x17FF	0	✓	×	✓	×	×	✓	×	×	✓	1
3	0x1800-0x1FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
4	0x2000-0x27FF	0	✓	×	✓	×	×	✓	×	×	✓	1
5	0x2800-0x2FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
6	0x3000-0x37FF	0	✓	×	✓	×	×	✓	×	×	✓	1
7	0x3800-0x3FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
8	0x4000-0x47FF	0	✓	×	✓	×	×	✓	×	×	✓	1
9	0x4800-0x4FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
10	0x5000-0x57FF	0	✓	×	✓	×	×	✓	×	×	✓	1
11	0x5800-0x5FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
12	0x6000-0x67FF	0	✓	×	✓	×	×	✓	×	×	✓	1
13	0x6800-0x6FFF	0	✓	×	✓	×	×	✓	×	×	✓	1
14	0x7000-0x77FF	0	✓	×	✓	×	×	✓	×	×	✓	1
15	0x7800-0x7FFF	0	✓	×	✓	×	×	✓	×	×	✓	1

NM = Normal

SW = SWD status

BOOT = BOOT status

BOOT partition protection: The 4KBytes space is divided into 4 segments, each segment is 1KBytes, and the protection status can be set separately in the user configuration register CFG_BOOTPE. If an APROM interval has been assigned, the protection state acts within the valid BOOT region.

Description of the boot area protection status												
bit	address	Valid status	Read			programming			Erase			Default value
			NM	SW	BT	NM	SW	BT	NM	SW	BT	-
0	0x7000-0x73FF	0	×	×	×	×	×	×	×	×	×	1
1	0x7400-0x77FF	0	×	×	×	×	×	×	×	×	×	1
2	0x7800-0x7BFF	0	×	×	×	×	×	×	×	×	×	1
3	0x7C00-0x7FFF	0	×	×	×	×	×	×	×	×	×	1

NM = Normal

SW = SWD status

BOOT = BOOT status

25.5 Procedure CRC check

25.5.1 CRC checksum calculation for Flash space

The chip supports the hardware calculation program CRC checksum. The FMC control module supports hardware to automatically calculate the value of CRC16. The check interval can be set arbitrarily. The CRC checksum is generated using the polynomial CRC-16-CCITT '$X^{16}+X^{12}+X^5+1$', The relevant registers are as follows:

FMCADR: The start address register for the CRC check

FMCCRCEA: The end address register for CRC checksum (FMCRCCEA>=FMCADR) is required

FMCCRCIN: Input register for CRC checking

FMCCRCD: Data register for CRC checking (holds 16-bit results of C RC checking).

The steps to calculate the CRC checksum are as follows:

1) Set the starting address of the required check space in FMCADR
2) Set the end address of the required check space in FMCCRCEA, which must be greater than or equal to FMCADR
3) Write FMCCRCIN to 0x00
4) Write FMCCRCD to 0x0000, clear the previous results
5) Write FMCCMD to 0xD and start the CRC checksum
6) After the CRC check is complete, the BUSY bit in FMCCON will be set to 0
7) Read the FMCCRCD data, that is, the calculated CRC checksum

During the Flash space check, the CPU stops, and after the calculation is complete, the CPU continues to run. The CRC check is checked bytely (8 bits), in order from the initial address to the end address.

For example, the data 0x0 address is 12H, the data at address 0x1 is 34H, the data at address 0x2 is 56H, and the data at address 0 x3 is 78 H, the value of CRC is calculated sequentially in the order of 12 H->34H->56H->78H, and the final check code is: 67F0H

Verifying 32KB of Bytes program space requires about 1ms@Fsys=48MHz.

The CRC check of the Flash space takes effect on the absolute address of flash and is not affected by the protected state, the BOOT state.

25.5.2 CRC checksum comparison for Flash space

The program CRC checksum is recommended to be generated using the polynomial CRC-16-CCITT of "$X^{16}+X^{12}+X^5+1$". This uses the same polynomial in FMC as the CRC module to quickly verify that the program code is correct. (CMS-related tool support is required when using this function).

There are two ways to read PCRCD:

1) Read by the FMC module, the corresponding address mapping is as follows:

(Memory address = 0x1000_0000) RO: read-only; WO: Write only; R/W: Read and write.

address	Offset	R/W	description	Reset value
PCRCD	0x01C	RO	PCRCD	-

2) Read by the system control module SYSCON, the corresponding address mapping is as follows:

(Register base address = 0x5000_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
PCRCD	0x510	RO	{ 16'h0， PCRCD }	-

25.6 CRC operation (general CRC)

The universal CRC module verifies the correctness of the program or data transmission. The CRC operations of the general-purpose module operate at the APB clock.

The polynomial of CRC is "X 16+X 12+X^5+1" of CRC-16-CCITT.

25.7 Memory illegal access detection

Access to the illegal memory address in the ARM microcontroller generates an error exception, which provides a better method of detecting program errors and allows software errors to be detected earlier.

In an AHB system connected to a Cortex-M0 processor, the address resolution logic probes for the address being accessed, and if an illegal location is being accessed, the bus system responds with an error signal that can cause a bus error by taking values or data access.

25.8 SRAM protection function

The on-chip SRAM is write-protected and can be set to zonal write-protected. Write protection does not affect the read function, the system register SRAMLOCK can set the relevant function.

25.8.1 SRAM write enable register (SRAMLOCK)

bit	symbol	description	Reset value
31:16	LOCK	When LOCK=0x55AA, the write protection of SRAM takes effect	0x0
15:4	-	Reserved	-
3:0	REGION	Bit3: Set the SRAM address 0x20001800-0x20001FFF area to write-protected Bit2: Set the SRAM address 0x20001000-0x200017FF area to write-protected Bit1: Set the SRAM address 0x20000800-0x20000FFF area to write-protected Bit0: - Write 0 to disable protection function (R/W) Write 1 to enable protection function (only reads allowed) Note: The 2KBytes area with an initial address range of 0x20000000-0x2000 07FF is free to read and write.	0x0

25.9 SFR protection function

Some SFRs of the key function modules have protection functions and can be set to level protection. The associated registers with SFR protection can be referred to the register mapping instructions for each module.

The protection level types are as follows:

Protection level	The type of protection	Description
0	P0	While Data is written, detect other register values at the same time (A569H/55AAH).
1	P1A	While Data is written, detect other register values (55H/AAH/99H).
2	P1B	While Data is written, detect other register values (55H).
3	P1C	While Data is written, detect other register values (55AAH).
4	P1D	While Data is written, detect other register values (55AA6699H).
5	P2	Reserved

For example, GPIO, IOCFG, WDT, FMC, CCP0/1, EPWM, ACMP0/1, Functional modules such as ADC0/1 have similar protection lock registers to implement the SFR protection function. For specific use, please refer to the user manual for each module.

25.10 ADC test function

This A/D test function verifies that the A/D converter is operating properly by converting the A/D converter's positive reference voltage, negative reference voltage, analog input channel (ANi), and internal reference voltage.

The ADC0/ADC1 support the test functions of the ADC.

25.11 GPIO pin voltage level detection

When the port is configured as a GPIO as the output port, the status of the pin can also be read. That is, it can detect the IO port as the output port, and can also detect whether the preset level value of the output is correct. In GPIO function mode, whether the port is configured as an output port or an input port, the pin level can be read via GPIO->DI.

Each set of GPIO input circuits supports filtering and is selectable in filter width. The GPIOxDIDB register determines whether to filter and the sample clock for filtering. The basic sample clock of the filter is HCLK, and a total of 8 sample clocks can be selected from HCLK-HCLK/14.

After three consecutive samples by the sample clock, if they are all at the same level, the pin level is considered stable. If it is not the same, the pin level is considered to be jittery, and the read value is the state of the level before jitter. The structure filters out glitches less than 2× Ts (sample clock cycle) widths.

26. User Configuration Area (UCFG)

26.1 overview

The user configuration area is a 128-word storage area allocated in FLASH, which reserves registers for the system and is used to configure the external reset IO multiplexing function, encryption function, userID and other information.

26.2 Register mapping

(Base address = 0x1000_0000) RO: read-only; WO: Write only; R/W: Read and write.

register	Offset	R/W	description	Reset value
Config0	0x000	RO	User configuration register 0	-
Config1	0x004	RO	User configuration register 1	-
Config2	0x010	RO	User configuration register 2	-
Config3	0x014	RO	User configuration register 3	-
INSRUID0	0x024	RO	The user's unique chip identification number ID0	-
INSRUID1	0x028	RO	The user's unique chip identification number ID1	-
INSRUID2	0x02c	RO	The user's unique chip identification number ID2	-

26.3 Register description

26.3.1 User Configuration Register 0 (Config0)

bit	symbol	description	Reset value
31:13	-	Reserved	-
12:11	Reset voltage selection bit	Reset voltage selection bit 10: 2.6V 01: 2.1V 00: 1.9V	-
10:8	-	Reserved	-
7:4	BOOT_TYPE	Program start position selection on power-on reset (requires allocation of validBOOT space). 1111: - 0011: Boot from APROM 0001: Boot from the BOOT area 0000: Start from the BOOT area, configure the BOOT pin as a dedicated port, and require the BOOT pin = 0. Other: Boot from APROM Note: Booting from theBOOT area requires allocating a valid BOOT space, otherwise booting from APROM.	-
3	-	Must be 0	-
2	USRIDPE	User UID encryption bit 1: Not encrypted 0: Encrypted	-
1	-	Must be 1	-
0	DATA-PROTECT	Encryption bits 1: Not encrypted 0: Encrypted	-

26.3.2 User Configuration Register 1 (Config1)

bit	symbol	description	Reset value
31:28	CONFIG_EN_WDT	WDT enable bit 1111: Power-on does not enable WDT Other: Power-on enables WDT	-
27:24	WDT_TIME	0000: 2ms（WDTLOAD=0x50） 0001: 4ms（WDTLOAD=0xA0） 0010: 8ms（WDTLOAD=0x140） 0011: 16ms（WDTLOAD=0x280） 0100: 32ms（WDTLOAD=0x500） 0101: 64ms（WDTLOAD=0xA00） 0110: 128ms（WDTLOAD=0x1400） 0111: 256ms（WDTLOAD=0x2800） 1000: 512ms（WDTLOAD=0x5000） 1001: 1024ms（WDTLOAD=0xA000） 1010: 1638ms（WDTLOAD=0xFFFF） 1011: 1638ms（WDTLOAD=0xFFFF） 1100: 1638ms（WDTLOAD=0xFFFF） 1101: 1638ms（WDTLOAD=0xFFFF） 1110: 1638ms（WDTLOAD=0xFFFF） 1111: 1638ms（WDTLOAD=0xFFFF）	-
23:14	-	Reserved	-
13:12	DEBUGEN	SWD debug enable bit 00: Disable Other: Enable	-
11:10	RESETIOS	External reset selection 11: External reset prohibits 10: P10 acts as an external reset port 01: P44 acts as an external reset port 00: P43 acts as an external reset port	-
9:0	-	Reserved	-

26.3.3 User Configuration Register 2 (Config2)

bit	symbol	description	Reset value
31:16	-	Reserved	-
15:0	USRAPE	APROM program space write protection bit (one segment every 2K). If a BOOT region is assigned, the Bit14, Bit15 bits act to the valid APROM region. The protection status is: SWD prohibits R/W/single page erase. Normally disables write/erase. BOOT program operations are not affected Bit0: 0x0000-0x07FF (absolute address of F LASH). Bit1: 0x0800-0x0FFF Bit2: 0x1000-0x17FF …… Bit14:0x7000-0x77FF Bit15: 0x7800-0x7FFF 0: protection 1: Not protected	-

26.3.4 User Configuration Register 3 (Config3)

bit	symbol	description	Reset value
31:20	-	Reserved	-
19:16	INSRBTS	APROM/BOOT space allocation bits 0000: APROM=28K； BOOT=4K 0001: APROM=30K； BOOT=2K 0010: APROM=31K； BOOT=1K Others: APROM=32K; BOOT=0K	-
15:4	-	-	-
3:0	USRBPE	BOOT program space write protection bit (one segment every 1K). If the BOOT region is less than 4K, the protective bit acts on the active BOOT region. The protection status is: SWD prohibits R/W/single page erase. Normal operation prohibits R/W/erase. The BOOT program prohibits reading/writing/erasing. Bit0: 0x7000-0x73FF (absolute address of F LASH). Bit1: 0x7400-0x77FF Bit2: 0x7800-0x7BFF Bit3: 0x7C00-0x7FFF 0: protection 1: Not protected	-

26.3.5 The user's unique chip identification number ID0 (USRUID0)

bit	symbol	description	Reset value
31:0	USRUID0	The user's unique chip identification number ID bit [31:0].	-

26.3.6 The user's unique chip identification number ID1 (USRUID1)

bit	symbol	description	Reset value
31:0	USRUID1	The user's unique chip identification number ID bit [63:32]	-

26.3.7 The user's unique chip identification number ID2 (USRUID2)

bit	symbol	description	Reset value
31:0	USRUID2	The user's unique chip identification number ID bit [95:64].	-

27. Version Revision Notes

Version number	Time	Revision Content
V1.00	April 2019	Initial release
V1.01	April 2020	Added user configuration area register description Modify the APBCKSEL/UARTxEFR/I2CCLK register description
V1.10	October 2021	Update the chip list
V1.11	December 2022	Modify the following register descriptions: 1) 15.5.10 CCP write enable control register (CCPLOCK) 2) 16.5.8 EPWM output control register (POEN) 3) 5.3.34 P30 configuration register (IOP30CFG)